CMS32M67xx Datasheet

Ultra-low power 32-bit microcontrollers based on ARM® Cortex®-M0+

128KB Flash, analog functions, Timers, and communication interfaces.

V1.0.1

Features

- **Ultra-low power operation environment**
  - Supply voltage range: 1.8V to 5.5V
  - Temperature range: -40℃ to 105℃
  - Low power consumption modes: sleep mode, deep sleep mode
  - Operating power consumption: 70μA/MHz@72MHz
  - Power consumption in deep sleep mode: 50μA
  - Power consumption in deep sleep mode with partial power down: 30μA
- **Core**
  - ARM®32-bitCortex®-M0+ CPU
  - Single-cycle hardware multiplier
- **32-bit hardware division unit (DIV)**
  - Division supports both signed and unsigned operations
- **32-bit hardware division and square root unit (DIVSQRT)**
  - Division and square root unit supports both signed and unsigned operations
- **Memory**
  - 128KB Flash memory
  - 1KB dedicated data Flash memory
  - 4KB SRAM0 memory and 8KB SRAM1 memory
- **Clock management**
  - High-speed oscillator (high-speed OCO): 72MHz/64MHz
  - Low-speed oscillator (low-speed OCO): 15KHz
  - X1 oscillation circuit: 4MHz~8MHz
  - PLL: X1 or high-speed OCO provides a clock signal after division, with a maximum output clock of 72 MHz and a minimum output clock of 48 MHz.
- **Power and reset management**
  - Power-on reset (POR)
  - Low voltage detection (LVD) (threshold voltage can be set)
- **Capture/Compare/Pulse Width Modulated Module (CCP0/1)**
  - Supports 4 PWM outputs with independently configurable periods.
  - CCP1 can simultaneously capture on 4 channels.
- **Enhanced PWM(EPWM)**
  - 8 channels
- **GPIO**
  - Up to 46 GPIOs with support for digital function assignment
  - Most GPIOs support pull-up/down resistor function
  - Some GPIOs support TTL/Schmitt inputs
- **Enhanced DMA**
  - The source/destination range can be selected for the entire address space.
  - Supports normal mode, repeat mode, and chain transfer.
  - Interrupt trigger for activation.
- **Rich timer resources**
  - Universal timer unit: 4 channels
  - 32/16bit timer: 2x
  - 12bit interval timer: 1x
  - Watchdog timer (WDT): 1x
  - SysTick timer: 1x
- **Rich and flexible interfaces**
  - UART: 2 channels
  - SSP/SPI: 1 channel (support 4 to 16 bits)
  - IICA: 1 channel
- **High-precision 12-bit ADC**
  - Up to 27 input channels
  - Each conversion channel has an independent result register
  - Supports one-shot/continuous mode
  - 1 comparator for conversion results, which can generate interrupts after conversion
  - Selectable reference voltage: VDD/4.2V/3.6V
- **Digital-to-Analog Converter (DAC)**
  - Selectable analog input voltage reference: VDD/4.2V/3.6V
  - Multi-level selectable output voltage
- **Programmable Gain Amplifier (PGA0/1/2/3)**
  - Selectable internal gains: 1 to 15x
  - Supports fully differential architecture
  - Selectable output modes
- **Analog Comparators (ACMP0/1)**
  - Multiple selectable positive terminals
  - Negative terminal can be input port or internal reference voltage
  - Supports selectable hysteresis voltage: 10mV/20mV/60mV

- Supports independent/complementary /synchronous/grouped output modes
- Supports edge-aligned and center-aligned modes
- Supports one-shot mode (edge alignment only) or auto-load mode
- Complementary PWM with programmable deadband generator support
- Supports masks and mask presets
- Supports Hall sensor interface
- Supports hardware brake and recovery function

◆ **HALL signal processing module**

- Supports 3 HALL sensor inputs

◆ **Serial debug interface SWD (2-Wire)**

- Both comparator outputs and generation events can trigger the EPWM brake

◆ **Safety features**

- Compliant with IEC60730 and IEC61508 standards
- Abnormal memory access error reporting
- Supports hardware CRC
- Supports protection of important SFRs to prevent misoperations
- 128-bit unique ID

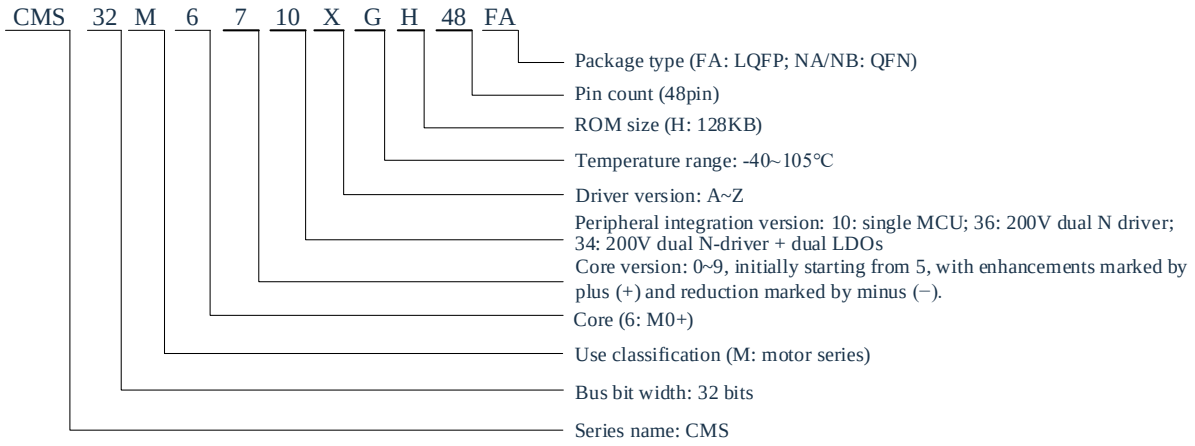
1. Overview

1.1 Introduction

The ultra-low power CMS32M67xx features a high-performance ARM® Cortex®-M0+ 32-bit microcontroller, capable of operating at up to 72 MHz. It incorporates high-speed embedded flash memory (SRAM0 up to 4KB, SRAM1 up to 8KB, and program/data flash up to 128KB). This product integrates various standard interfaces such as I^2C, SPI, and UART. It also includes a 12-bit A/D converter, a DAC, a programmable gain amplifier (PGA), an analog comparator (ACMP), and a temperature sensor. The 12-bit A/D converter allows for the acquisition of external sensor signals, reducing system design costs. The integrated temperature sensor enables real-time monitoring of the external environment's temperature. The chip also integrates a watchdog timer, universal timers (Timer0/1), an universal timer unit, and a 12-bit interval timer (LSITIMER), meeting various clock requirements under different conditions. Additionally, it includes capture/compare/pulse modulation units, a divider unit, a division and square root unit, an enhanced PWM module, an advanced DMA, and a Hall signal processing module.

The CMS32M67xx offers exceptional low-power performance and supports two low-power modes: sleep and deep sleep, providing flexible design options.

1.2 Product Model List



Product list of CMS32M67xx:

Product model	Flash memory	Dedicated data Flash memory	SRAM	Package
CMS32M6710GH32NB	128KB	1KB	12KB	32-pin plastic QFN32 (4.0x4.0mm, 0.4mm pitch)
CMS32M6710GH48FA	128KB	1KB	12KB	48-pin plastic LQFP48 (7.0x7.0mm, 0.5mm pitch)
CMS32M6736EGH48NB	128KB	1KB	12KB	48-pin plastic QFN48 (6.0x6.0mm, 0.4mm pitch)
CMS32M6736EGH48FA	128KB	1KB	12KB	48-pin plastic LQFP48 (7.0x7.0mm, 0.5mm pitch)
CMS32M6734EGH48FA	128KB	1KB	12KB	48-pin plastic LQFP48 (7.0x7.0mm, 0.5mm pitch)

1.3 Product Comparison

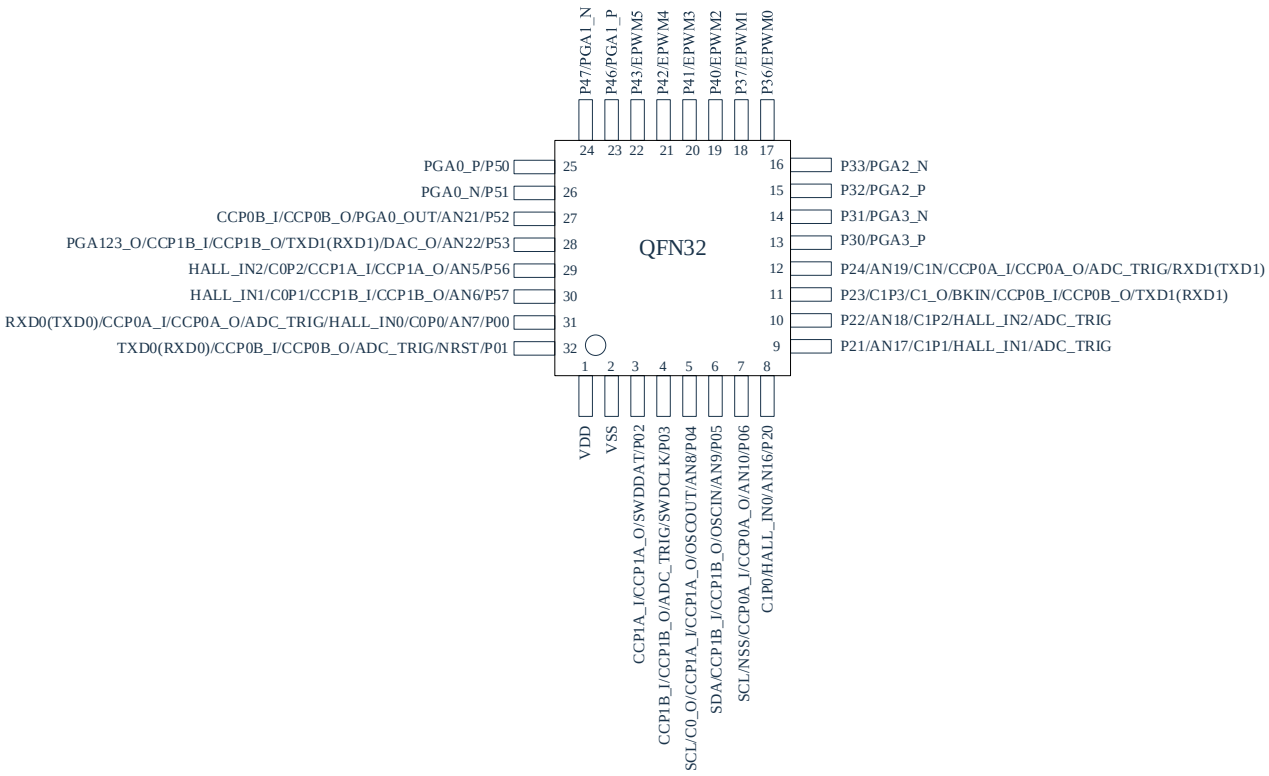
The following is a product comparison of the CMS32M67xx chip:

Peripheral interface \ Product model		CMS32M6710 GH32NB	CMS32M6710 GH48FA	CMS32M6736EG H48NB	CMS32M6736EG H48FA	CMS32M6734E GH48FA
Internal driver supply voltage		-	-	5~20V	5~20V	5~20V
Gate driver		-	-	6N	6N	6N
Internal LDO		-	-	-	-	5V+12V
Driver power supply withstand voltage		-	-	25V	25V	25V
High-side floating VS port withstand voltage		-	-	200V	200V	200V
MCU operating voltage		1.8V~5.5V				
Maximum clock frequency		72MHz				
Memory	ROM	128KB				
	Data Flash	1KB				
	SRAM	12KB				
Timer	SysTick	1				
	WDT	1				
	TIMER0/1	2				
	TAU (Number of channels)	4				
Enhanced digital peripheral	CRC	1				
	DIV	1				
	DIVSQRT	1				
	CCP	2				
	EPWM (Number of channels)	6	8	6	6	6
	DMA	1				
	HALL signal processing	1				
Comm. interface	UART	2				
	IICA	1				
	SSP/SPI	1				
Analog module	12bit-ADC (Number of channels)	21	27	25	25	22
	DAC	1				
	ACMP	2				
	PGA	4				3

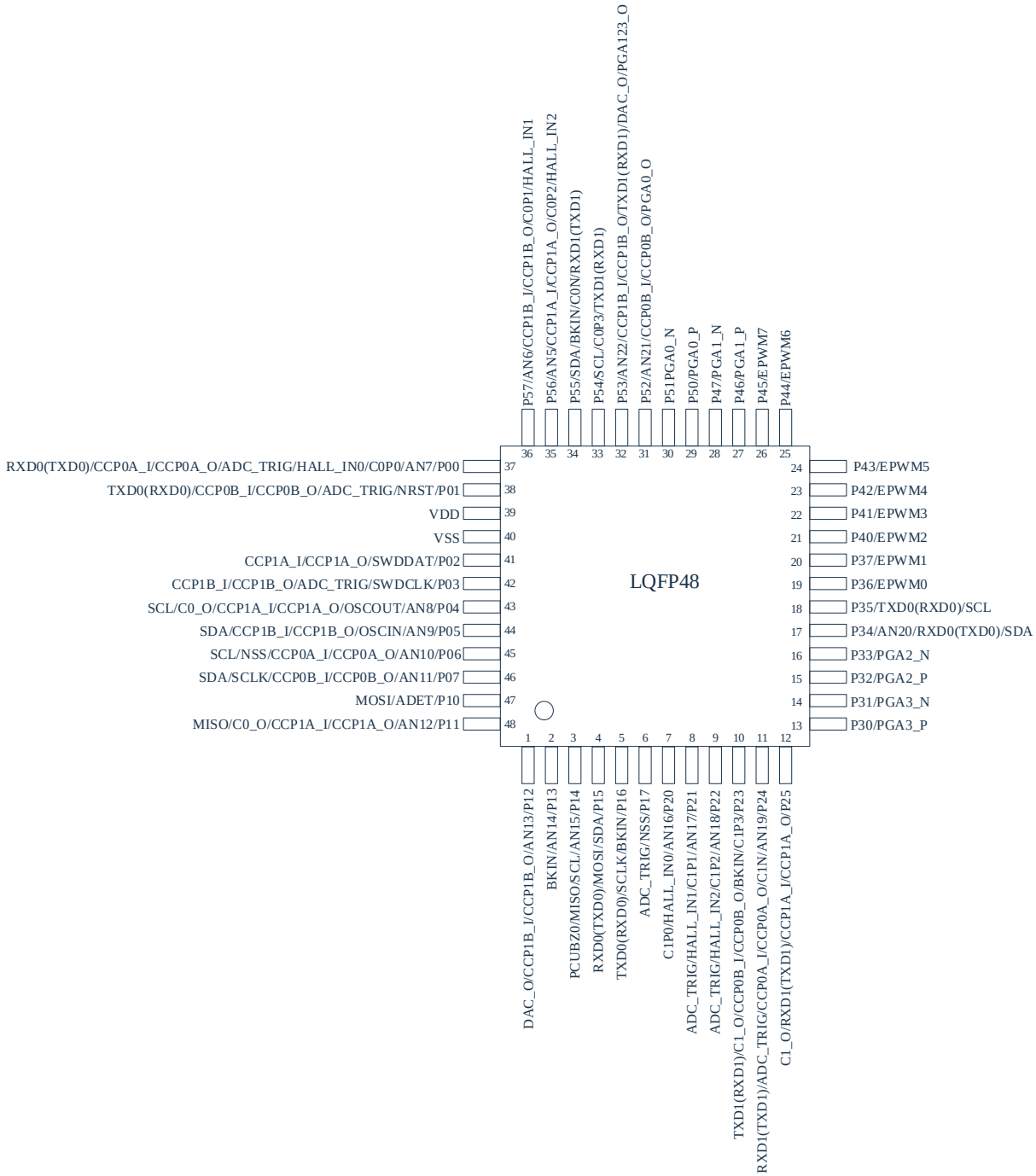
GPIOs	30	46	32	32	26
Operating temperature	-40~105℃				
Package	QFN32	LQFP48	QFN48	LQFP48	LQFP48

1.4Top View

1.4.1 CMS32M6710GH32NB

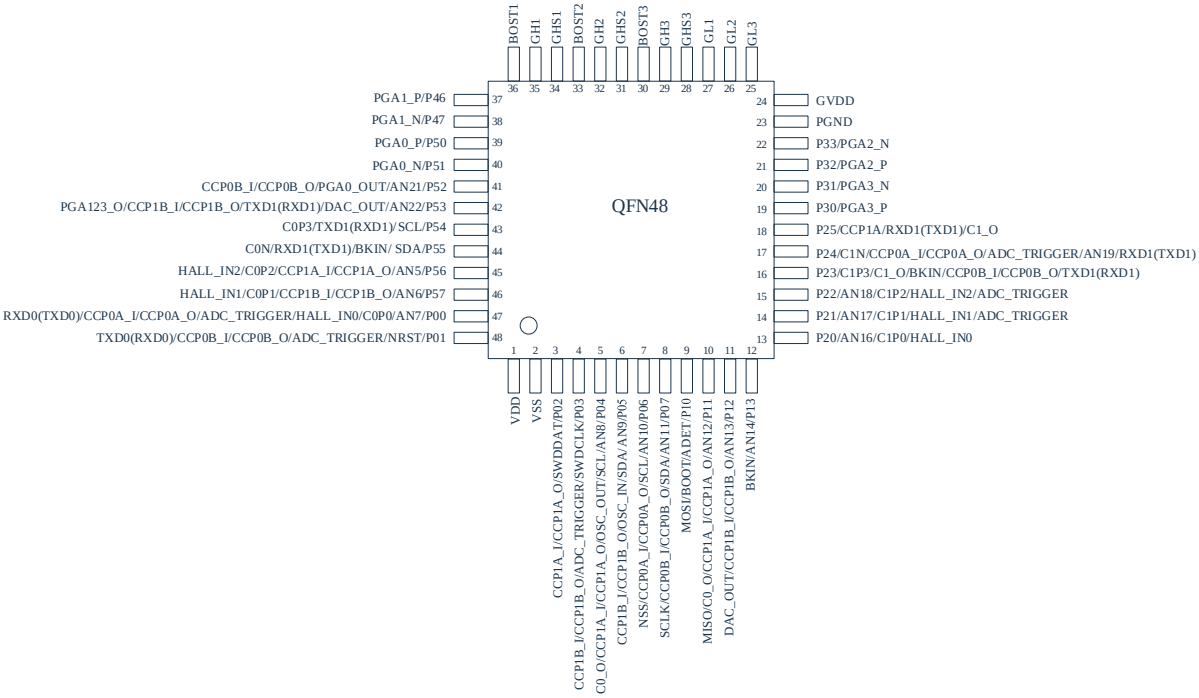


1.4.2 CMS32M6710GH48FA

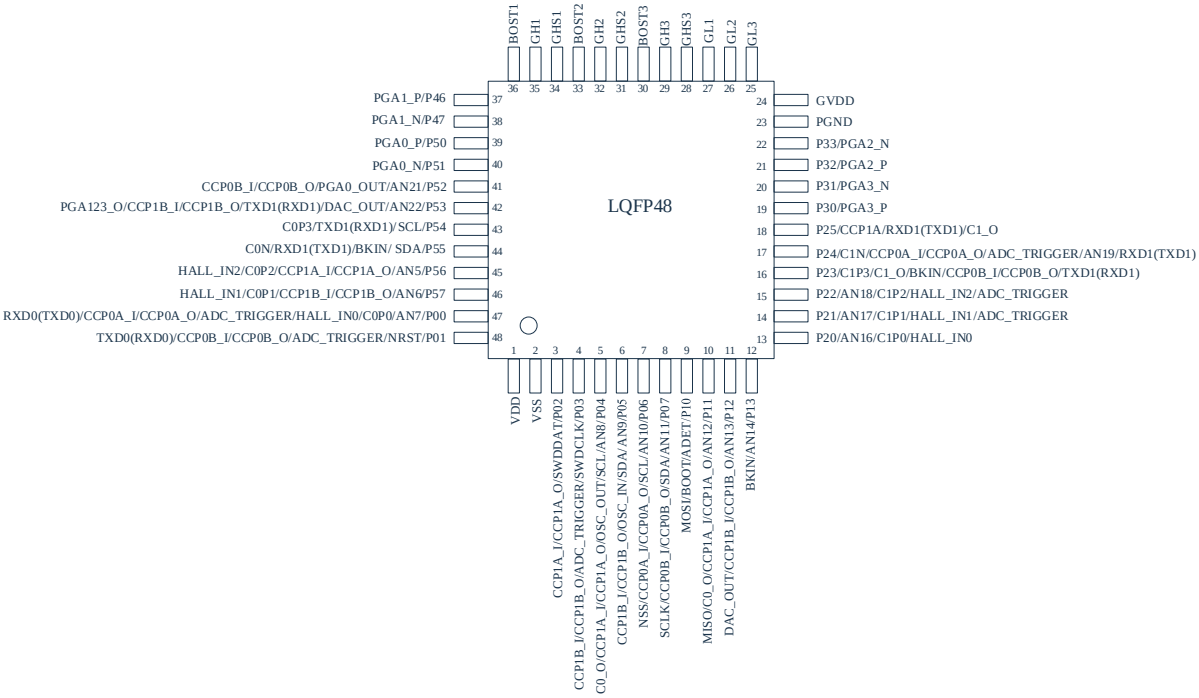


Note: INTP0, INTP1, INTP2, INTP3, TI00, TI01, TI02, TI03 can be mapped to any GPIO.

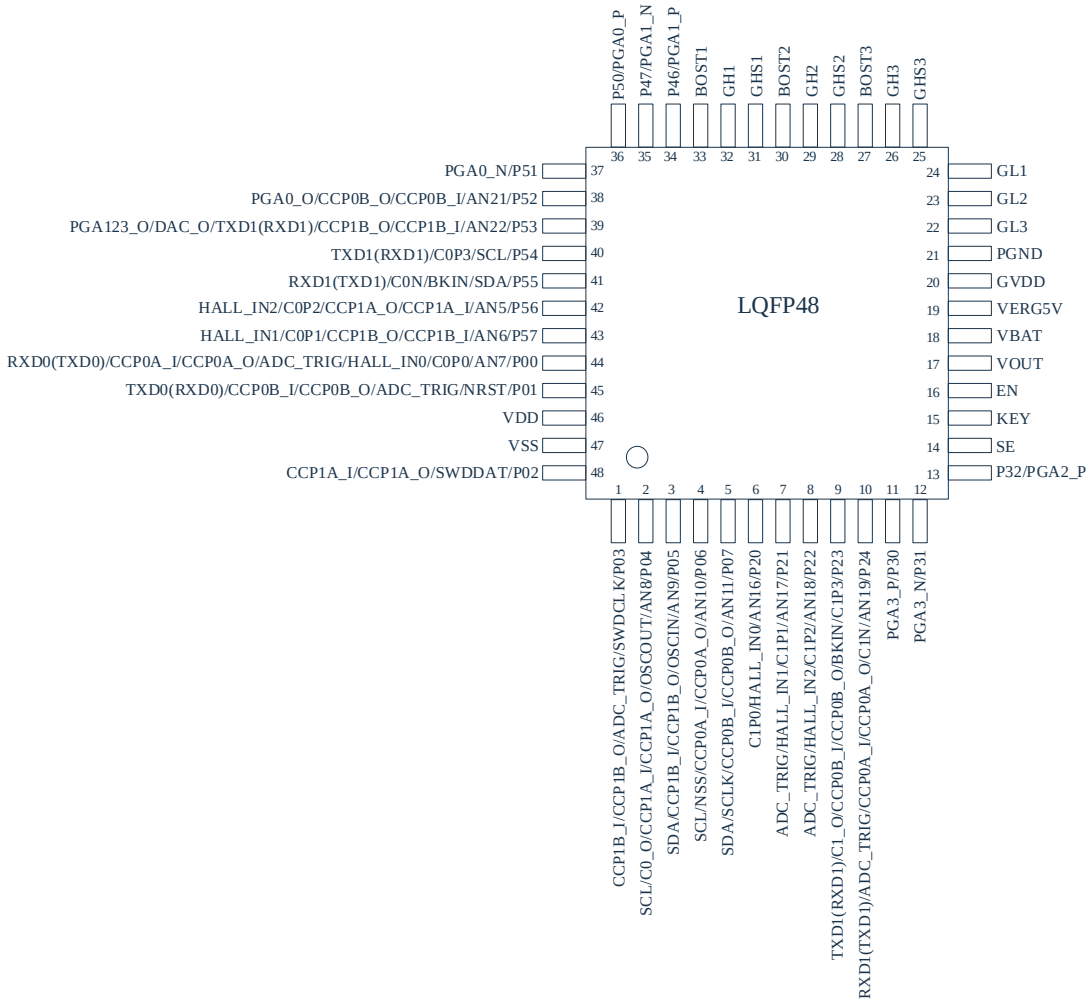
1.4.3 CMS32M6736EGH48NB



1.4.4 CMS32M6736EGH48FA

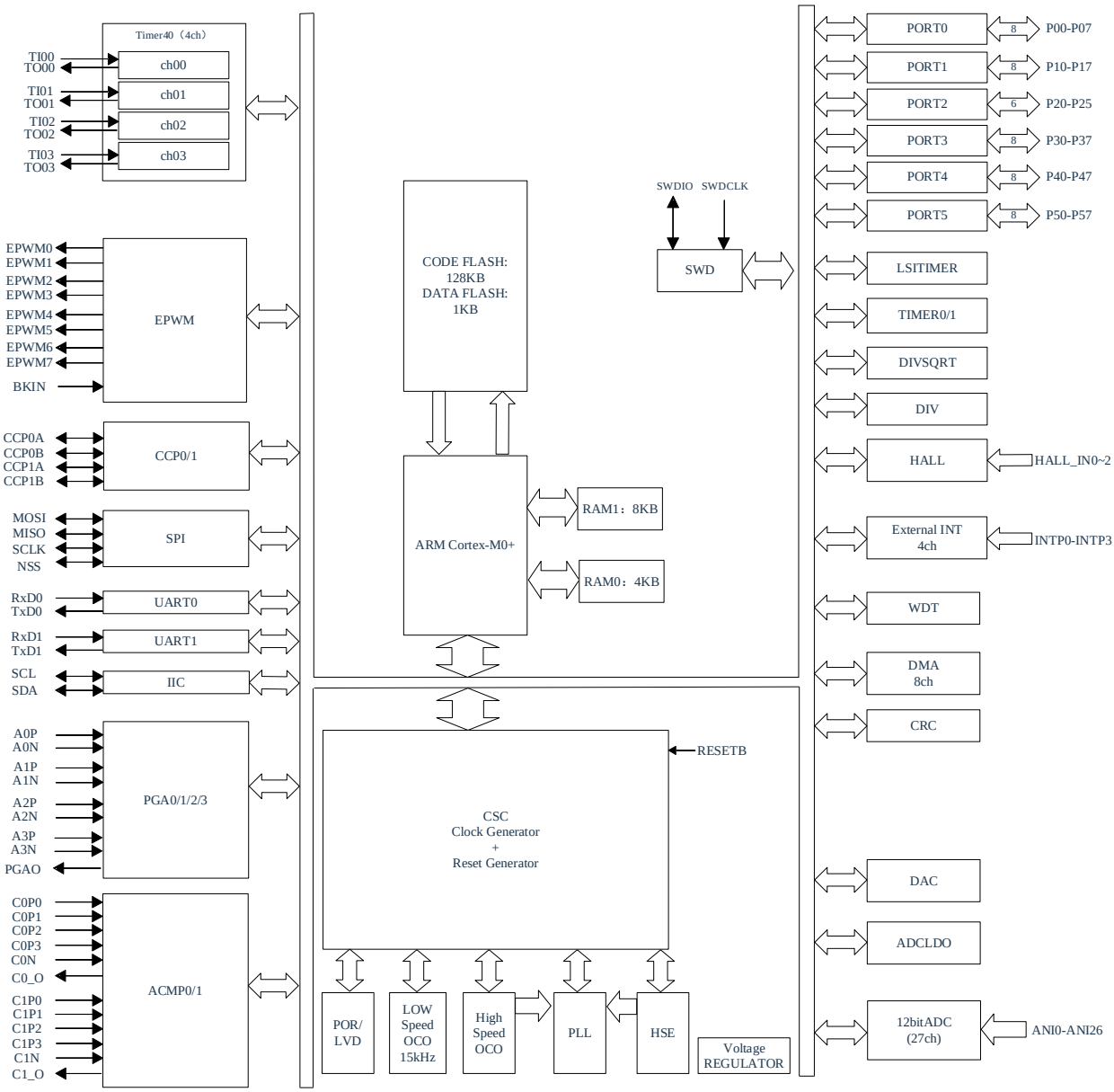


1.4.5 CMS32M6734EGH48FA

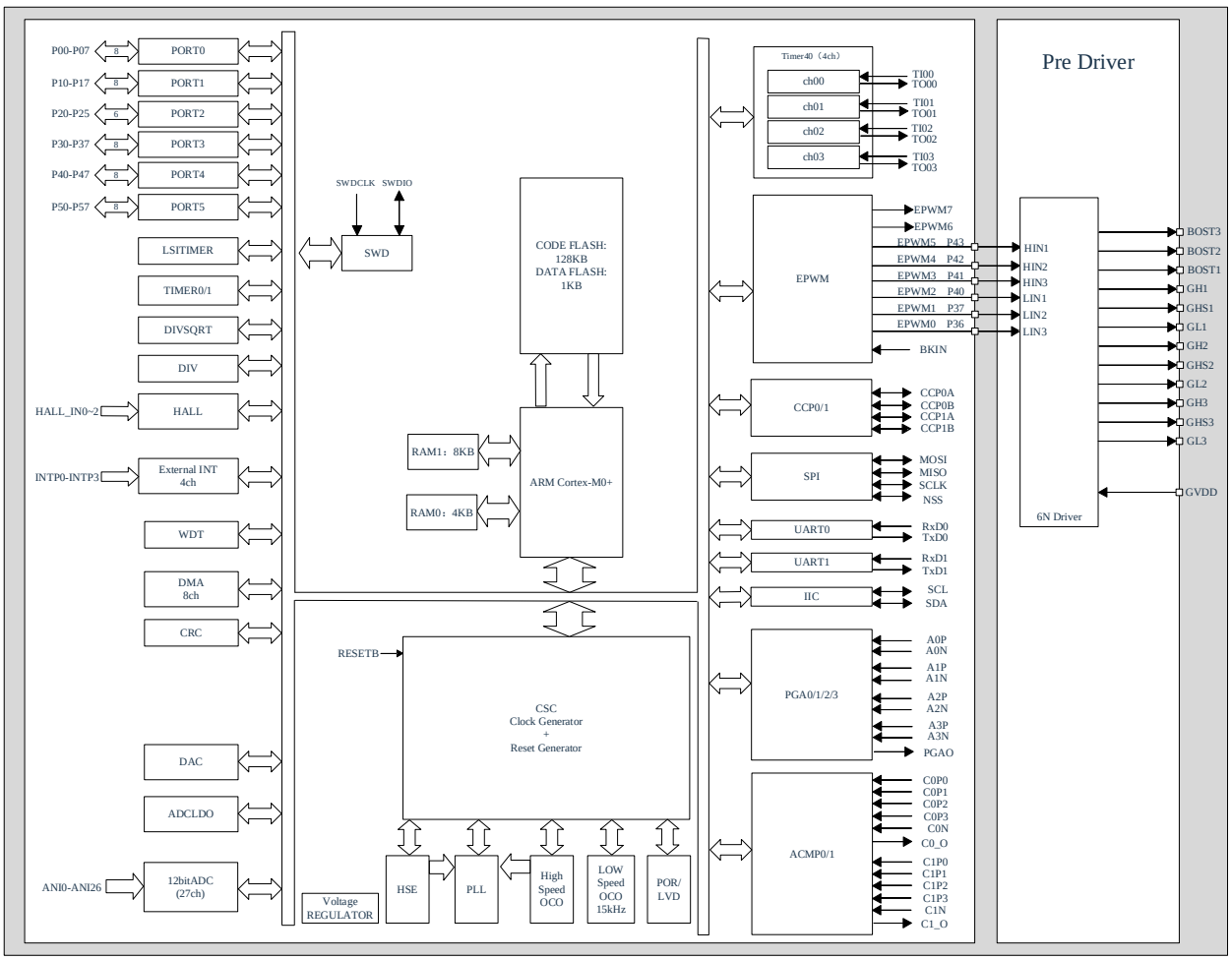


2. Product Block Diagrams

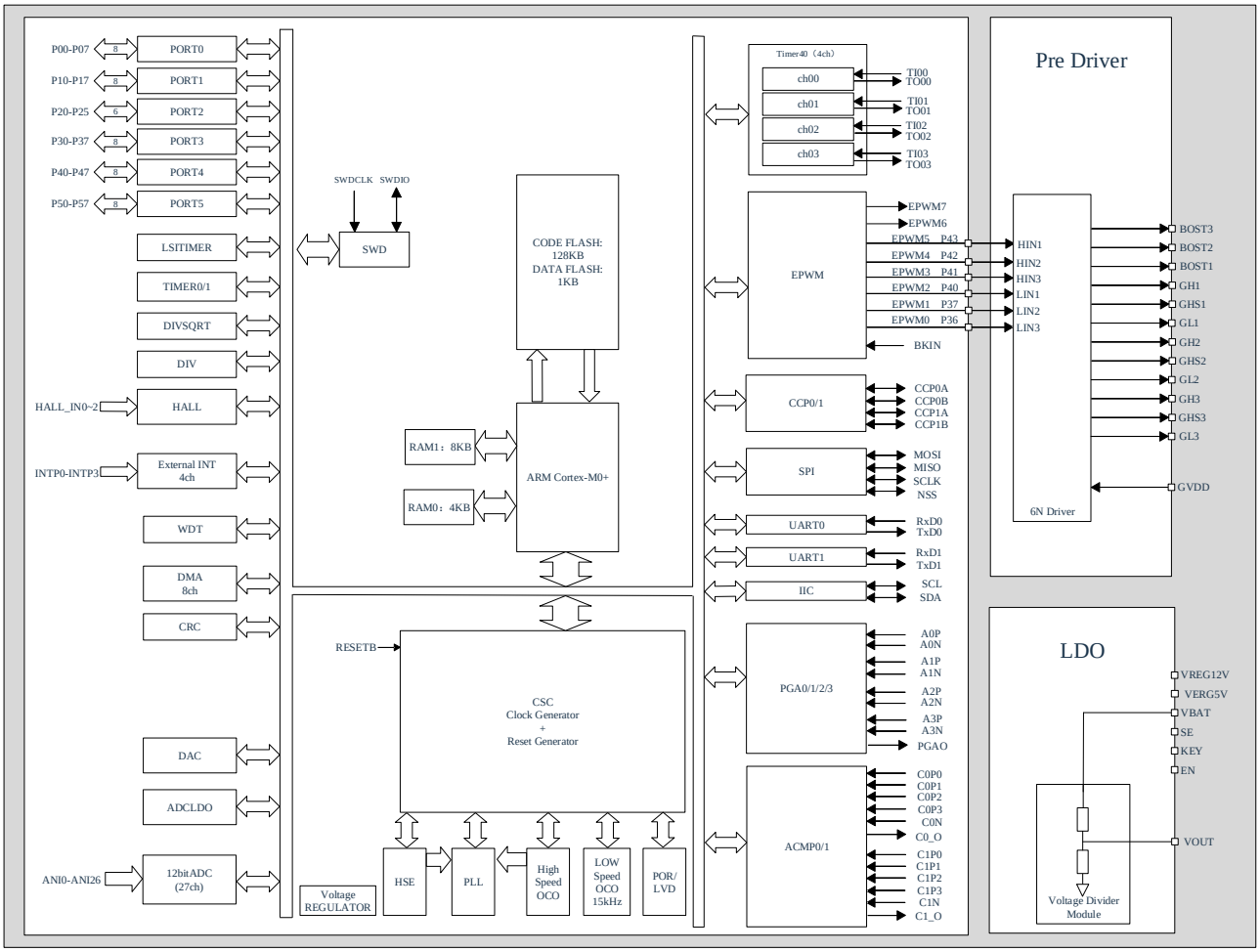
2.1 CMS32M6710GH48FA/CMS32M6710GH32NB



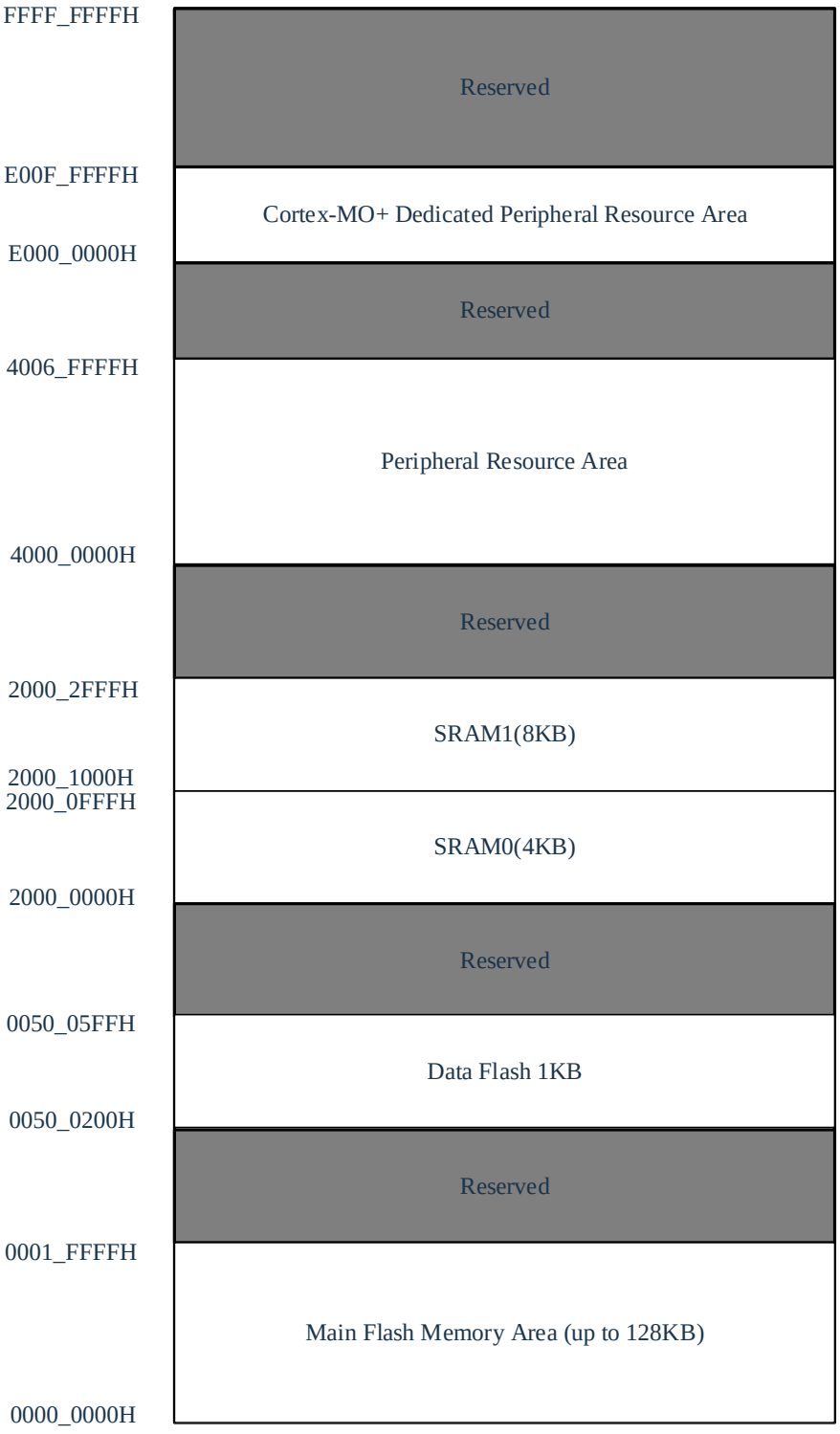
2.2 CMS32M6736EGH48NB/CMS32M6736EGH48FA



2.3 CMS32M6734EGH48FA



3. System Address Mapping



4. Pin Functions

4.1 CMS32M6710GH32NB

The symbols in the table below are described as follows:

Pin name	Symbol description
I/O	Digital input/output
I	Digital input
O	Digital output
AI	Analog input
AO	Analog output
P	Power or ground

Pin number	Pin name	Pin type	Description
3	P02	I/O	GPIO is configured for input, output, pull-up, pull-down, and other functions through registers.
	SWDDAT	I/O	SWD data port
	CCP1A_I	I	CCP1 capture input A pin
	CCP1A_O	O	CCP1 PWM output A pin
4	P03	I/O	GPIO is configured for input, output, pull-up, pull-down, and other functions through registers.
	SWDCLK	I	SWD clock port
	ADC_TRIG	O	ADC module trigger signal output pin
	CCP1B_I	I	CCP1 capture input B pin
	CCP1B_O	O	CCP1 PWM output B pin
5	P04	I/O	GPIO is configured for input, output, pull-up, pull-down, and other functions through registers.
	AN8	AI	ADC channel 8 input
	CCP1A_I	I	CCP1 capture input A pin
	CCP1A_O	O	CCP1 PWM output A pin
	OSCOUT	O	External crystal oscillator output port
	C0_O	O	ACMP0 output channel
	SCL	I/O	I2C clock input/output pin
6	P05	I/O	GPIO is configured for input, output, pull-up, pull-down, and other functions through registers.
	AN9	AI	ADC channel 9 input
	OSCIN	I	External crystal oscillator input port
	CCP1B_I	I	CCP1 capture input B pin
	CCP1B_O	O	CCP1 PWM output B pin
	SDA	I/O	I2C data input/output pin
7	P06	I/O	GPIO is configured for input, output, pull-up, pull-down, and other functions through registers.

Pin number	Pin name	Pin type	Description
	AN10	AI	ADC channel 10 input
	CCP0A_I	I	CCP0 capture input A pin
	CCP0A_O	O	CCP0 PWM output A pin
	NSS	I/O	SPI chip select pin
	SCL	I/O	I2C clock input/output pin
8	P20	I/O	GPIO is configured for input, output, pull-up, pull-down, and other functions through registers.
	AN16	AI	ADC channel 16 input
	C1P0	AI	ACMP1 positive input channel 0
	HALL_IN0	I	HALL input channel 0
9	P21	I/O	GPIO is configured for input, output, pull-up, pull-down, and other functions through registers.
	AN17	AI	ADC channel 17 input
	C1P1	AI	ACMP1 positive input channel 1
	ADC_TRIG	O	ADC module trigger signal output pin
	HALL_IN1	I	HALL input channel 1
10	P22	I/O	GPIO is configured for input, output, pull-up, pull-down, and other functions through registers.
	AN18	AI	ADC channel 18 input
	C1P2	AI	ACMP1 positive input channel 2
	ADC_TRIG	O	ADC module trigger signal output pin
	HALL_IN2	I	HALL input channel 2
11	P23	I/O	GPIO is configured for input, output, pull-up, pull-down, and other functions through registers.
	C1P3	AI	ACMP1 positive input channel 3
	C1_O	O	ACMP1 output channel
	BKIN	I	EPWM external brake signal input
	CCP0B_I	I	CCP0 capture input B pin
	CCP0B_O	O	CCP0 PWM output B pin
	RXD1	I	UART1 data input pin
	TXD1	O	UART1 data output pin
12	P24	I/O	GPIO is configured for input, output, pull-up, pull-down, and other functions through registers.
	AN19	AI	ADC channel 19 input
	C1N	AI	ACMP1 negative input channel
	CCP0A_I	I	CCP0 capture input A pin
	CCP0A_O	O	CCP0 PWM output A pin
	ADC_TRIG	O	ADC module trigger signal output pin
	RXD1	I	UART1 data input pin
	TXD1	O	UART1 data output pin
13	P30	I/O	GPIO is configured for input, output, pull-up, pull-down, and other functions through registers.

Pin number	Pin name	Pin type	Description
	PGA3_P	AI	PGA3 positive input channel
14	P31	I/O	GPIO is configured for input, output, pull-up, pull-down, and other functions through registers.
	PGA3_N	AI	PGA3 negative input channel
15	P32	I/O	GPIO is configured for input, output, pull-up, pull-down, and other functions through registers.
	PGA2_P	AI	PGA2 positive input channel
16	P33	I/O	GPIO is configured for input, output, pull-up, pull-down, and other functions through registers.
	PGA2_N	AI	PGA2 negative input channel
17	P36	I/O	GPIO is configured for input, output, pull-up, pull-down, and other functions through registers.
	EPWM0	O	EPWM output channel0
18	P37	I/O	GPIO is configured for input, output, pull-up, pull-down, and other functions through registers.
	EPWM1	O	EPWM output channel1
19	P40	I/O	GPIO is configured for input, output, pull-up, pull-down, and other functions through registers.
	EPWM2	O	EPWM output channel2
20	P41	I/O	GPIO is configured for input, output, pull-up, pull-down, and other functions through registers.
	EPWM3	O	EPWM output channel3
21	P42	I/O	GPIO is configured for input, output, pull-up, pull-down, and other functions through registers.
	EPWM4	O	EPWM output channel4
22	P43	I/O	GPIO is configured for input, output, pull-up, pull-down, and other functions through registers.
	EPWM5	O	EPWM output channel5
23	P46	I/O	GPIO is configured for input, output, pull-up, pull-down, and other functions through registers.
	PGA1_P	AI	PGA1 positive input channel
24	P47	I/O	GPIO is configured for input, output, pull-up, pull-down, and other functions through registers.
	PGA1_N	AI	PGA1 negative input channel
25	P50	I/O	GPIO is configured for input, output, pull-up, pull-down, and other functions through registers.
	PGA0_P	AI	PGA0 positive input channel
26	P51	I/O	GPIO is configured for input, output, pull-up, pull-down, and other functions through registers.
	PGA0_N	AI	PGA0 negative input channel
27	P52	I/O	GPIO is configured for input, output, pull-up, pull-down, and other functions through registers.

Pin number	Pin name	Pin type	Description
	AN21	AI	ADC channel 21 input
	CCP0B_I	I	CCP0 capture input B pin
	CCP0B_O	O	CCP0 PWM output B pin
	PGA0_O	AO	PGA0 output channel
28	P53	I/O	GPIO is configured for input, output, pull-up, pull-down, and other functions through registers.
	AN22	AI	ADC channel 22 input
	CCP1B_I	I	CCP1 capture input B pin
	CCP1B_O	O	CCP1 PWM output B pin
	RXD1	I	UART1 data input pin
	TXD1	O	UART1 data output pin
	PGA123_O	AO	PGA123 output channel
	DAC_O	AO	DAC voltage output channel
29	P56	I/O	GPIO is configured for input, output, pull-up, pull-down, and other functions through registers.
	AN5	AI	ADC channel 5 input
	CCP1A_I	I	CCP1 capture input A pin
	CCP1A_O	O	CCP1 PWM output A pin
	C0P2	AI	ACMP0 positive input channel2
	HALL_IN2	I	HALL input channel 2
30	P57	I/O	GPIO is configured for input, output, pull-up, pull-down, and other functions through registers.
	AN6	AI	ADC channel 6 input
	CCP1B_I	I	CCP1 capture input B pin
	CCP1B_O	O	CCP1 PWM output B pin
	C0P1	AI	ACMP0 positive input channel1
	HALL_IN1	I	HALL input channel 1
31	P00	I/O	GPIO is configured for input, output, pull-up, pull-down, and other functions through registers.
	AN7	AI	ADC channel 7 input
	C0P0	AI	ACMP0 positive input channel0
	HALL_IN0	I	HALL input channel 0
	ADC_TRIG	O	ADC module trigger signal output pin
	CCP0A_I	I	CCP0 capture input A pin
	CCP0A_O	O	CCP0 PWM output A pin
	RXD0	I	UART0 data input pin
	TXD0	O	UART0 data output pin
32	P01	I/O	GPIO is configured for input, output, pull-up, pull-down, and other functions through registers.
	NRST	I	External reset pin
	ADC_TRIG	O	ADC module trigger signal output pin
	CCP0B_I	I	CCP0 capture input B pin

Pin number	Pin name	Pin type	Description
	CCP0B_O	O	CCP0 PWM output B pin
	RXD0	I	UART0 data input pin
	TXD0	O	UART0 data output pin
1	VDD	P	Power supply
2	VSS	P	Ground

4.2 CMS32M6710GH48FA

The symbols in the table below are described as follows:

Pin name	Symbol description
I/O	Digital input/output
I	Digital input
O	Digital output
AI	Analog input
AO	Analog output
P	Power or ground

Pin number	Pin name	Pin type	Description
41	P02	I/O	GPIO is configured for input, output, pull-up, pull-down, and other functions through registers.
	SWDDAT	I/O	SWD data port
	CCP1A_I	I	CCP1 capture input A pin
	CCP1A_O	O	CCP1 PWM output A pin
42	P03	I/O	GPIO is configured for input, output, pull-up, pull-down, and other functions through registers.
	SWDCLK	I	SWD clock port
	ADC_TRIG	O	ADC module trigger signal output pin
	CCP1B_I	I	CCP1 capture input B pin
	CCP1B_O	O	CCP1 PWM output B pin
43	P04	I/O	GPIO is configured for input, output, pull-up, pull-down, and other functions through registers.
	AN8	AI	ADC channel 8 input
	CCP1A_I	I	CCP1 capture input A pin
	CCP1A_O	O	CCP1 PWM output A pin
	OSCOUT	O	External crystal oscillator output port
	C0_O	O	ACMP0 output channel
	SCL	I/O	I2C clock input/output pin
44	P05	I/O	GPIO is configured for input, output, pull-up, pull-down, and other functions through registers.
	AN9	AI	ADC channel 9 input
	OSCIN	I	External crystal oscillator input port
	CCP1B_I	I	CCP1 capture input B pin
	CCP1B_O	O	CCP1 PWM output B pin
	SDA	I/O	I2C data input/output pin
45	P06	I/O	GPIO is configured for input, output, pull-up, pull-down, and other functions through registers.
	AN10	AI	ADC channel 10 input
	CCP0A_I	I	CCP0 capture input A pin

Pin number	Pin name	Pin type	Description
	CCP0A_O	O	CCP0 PWM output A pin
	NSS	I/O	SPI chip select pin
	SCL	I/O	I2C clock input/output pin
46	P07	I/O	GPIO is configured for input, output, pull-up, pull-down, and other functions through registers.
	AN11	AI	ADC channel 11 input
	CCP0B_I	I	CCP0 capture input B pin
	CCP0B_O	O	CCP0 PWM output B pin
	SCLK	I/O	SPI clock input/output pin
	SDA	I/O	I2C data input/output pin
47	P10	I/O	GPIO is configured for input, output, pull-up, pull-down, and other functions through registers.
	ADET	I	ADC external trigger signal input channel
	MOSI	I/O	SPI master output/slave input pin
48	P11	I/O	GPIO is configured for input, output, pull-up, pull-down, and other functions through registers.
	AN12	AI	ADC channel 12 input
	CCP1A_I	I	CCP1 capture input A pin
	CCP1A_O	O	CCP1 PWM output A pin
	C0_O	O	ACMP0 output channel
	MISO	I/O	SPI master input/slave output pin
1	P12	I/O	GPIO is configured for input, output, pull-up, pull-down, and other functions through registers.
	AN13	AI	ADC channel 13 input
	CCP1B_I	I	CCP1 capture input B pin
	CCP1B_O	O	CCP1 PWM output B pin
	DAC_O	AO	DAC output channel
2	P13	I/O	GPIO is configured for input, output, pull-up, pull-down, and other functions through registers.
	AN14	AI	ADC channel 14 input
	BKIN	I	EPWM external brake signal input
3	P14	I/O	GPIO is configured for input, output, pull-up, pull-down, and other functions through registers.
	AN15	AI	ADC channel 15 input
	SCL	I/O	I2C clock input/output pin
	MISO	I/O	SPI master input/slave output pin
	PCUBZ0	O	Clock output/buzzer output pin 0
4	P15	I/O	GPIO is configured for input, output, pull-up, pull-down, and other functions through registers.
	SDA	I/O	I2C data input/output pin
	MOSI	I/O	SPI master output/slave input pin
	RXD0	I	UART0 data input pin

Pin number	Pin name	Pin type	Description
	TXD0	O	UART0 data output pin
5	P16	I/O	GPIO is configured for input, output, pull-up, pull-down, and other functions through registers.
	BKIN	I	EPWM external brake signal input
	SCLK	I/O	SPI clock input/output pin
	RXD0	I	UART0 data input pin
	TXD0	O	UART0 data output pin
6	P17	I/O	GPIO is configured for input, output, pull-up, pull-down, and other functions through registers.
	NSS	I/O	SPI chip select pin
	ADC_TRIG	O	ADC module trigger signal output pin
7	P20	I/O	GPIO is configured for input, output, pull-up, pull-down, and other functions through registers.
	AN16	AI	ADC channel 16 input
	C1P0	AI	ACMP1 positive input channel 0
	HALL_IN0	I	HALL input channel 0
8	P21	I/O	GPIO is configured for input, output, pull-up, pull-down, and other functions through registers.
	AN17	AI	ADC channel 17 input
	C1P1	AI	ACMP1 positive input channel 1
	ADC_TRIG	O	ADC module trigger signal output pin
	HALL_IN1	I	HALL input channel 1
9	P22	I/O	GPIO is configured for input, output, pull-up, pull-down, and other functions through registers.
	AN18	AI	ADC channel 18 input
	C1P2	AI	ACMP1 positive input channel 2
	ADC_TRIG	O	ADC module trigger signal output pin
	HALL_IN2	I	HALL input channel 2
10	P23	I/O	GPIO is configured for input, output, pull-up, pull-down, and other functions through registers.
	C1P3	AI	ACMP1 positive input channel 3
	C1_O	O	ACMP1 output channel
	BKIN	I	EPWM external brake signal input
	CCP0B_I	I	CCP0 capture input B pin
	CCP0B_O	O	CCP0 PWM output B pin
	RXD1	I	UART1 data input pin
	TXD1	O	UART1 data output pin
11	P24	I/O	GPIO is configured for input, output, pull-up, pull-down, and other functions through registers.
	AN19	AI	ADC channel 19 input
	C1N	AI	ACMP1 negative input channel
	CCP0A_I	I	CCP0 capture input A pin

Pin number	Pin name	Pin type	Description
	CCP0A_O	O	CCP0 PWM output A pin
	ADC_TRIG	O	ADC module trigger signal output pin
	RXD1	I	UART1 data input pin
	TXD1	O	UART1 data output pin
12	P25	I/O	GPIO is configured for input, output, pull-up, pull-down, and other functions through registers.
	CCP1A_I	I	CCP1 capture input A pin
	CCP1A_O	O	CCP1 PWM output A pin
	RXD1	I	UART1 data input pin
	TXD1	O	UART1 data output pin
	C1_O	O	ACMP1 output channel
13	P30	I/O	GPIO is configured for input, output, pull-up, pull-down, and other functions through registers.
	PGA3_P	AI	PGA3 positive input channel
14	P31	I/O	GPIO is configured for input, output, pull-up, pull-down, and other functions through registers.
	PGA3_N	AI	PGA3 negative input channel
15	P32	I/O	GPIO is configured for input, output, pull-up, pull-down, and other functions through registers.
	PGA2_P	AI	PGA2 positive input channel
16	P33	I/O	GPIO is configured for input, output, pull-up, pull-down, and other functions through registers.
	PGA2_N	AI	PGA2 negative input channel
17	P34	I/O	GPIO is configured for input, output, pull-up, pull-down, and other functions through registers.
	AN20	AI	ADC channel 20 input
	SDA	I/O	I2C data input/output pin
	RXD0	I	UART0 data input pin
	TXD0	O	UART0 data output pin
18	P35	I/O	GPIO is configured for input, output, pull-up, pull-down, and other functions through registers.
	SCL	I/O	I2C clock input/output pin
	RXD0	I	UART0 data input pin
	TXD0	O	UART0 data output pin
19	P36	I/O	GPIO is configured for input, output, pull-up, pull-down, and other functions through registers.
	EPWM0	O	EPWM output channel0
20	P37	I/O	GPIO is configured for input, output, pull-up, pull-down, and other functions through registers.
	EPWM1	O	EPWM output channel1
21	P40	I/O	GPIO is configured for input, output, pull-up, pull-down, and other functions through registers.

Pin number	Pin name	Pin type	Description
	EPWM2	O	EPWM output channel2
22	P41	I/O	GPIO is configured for input, output, pull-up, pull-down, and other functions through registers.
	EPWM3	O	EPWM output channel3
23	P42	I/O	GPIO is configured for input, output, pull-up, pull-down, and other functions through registers.
	EPWM4	O	EPWM output channel4
24	P43	I/O	GPIO is configured for input, output, pull-up, pull-down, and other functions through registers.
	EPWM5	O	EPWM output channel5
25	P44	I/O	GPIO is configured for input, output, pull-up, pull-down, and other functions through registers.
	EPWM6	O	EPWM output channel6
26	P45	I/O	GPIO is configured for input, output, pull-up, pull-down, and other functions through registers.
	EPWM7	O	EPWM output channel7
27	P46	I/O	GPIO is configured for input, output, pull-up, pull-down, and other functions through registers.
	PGA1_P	AI	PGA1 positive input channel
28	P47	I/O	GPIO is configured for input, output, pull-up, pull-down, and other functions through registers.
	PGA1_N	AI	PGA1 negative input channel
29	P50	I/O	GPIO is configured for input, output, pull-up, pull-down, and other functions through registers.
	PGA0_P	AI	PGA0 positive input channel
30	P51	I/O	GPIO is configured for input, output, pull-up, pull-down, and other functions through registers.
	PGA0_N	AI	PGA0 negative input channel
31	P52	I/O	GPIO is configured for input, output, pull-up, pull-down, and other functions through registers.
	AN21	AI	ADC channel 21 input
	CCP0B_I	I	CCP0 capture input B pin
	CCP0B_O	O	CCP0 PWM output B pin
	PGA0_O	AO	PGA0 output channel
32	P53	I/O	GPIO is configured for input, output, pull-up, pull-down, and other functions through registers.
	AN22	AI	ADC channel 22 input
	CCP1B_I	I	CCP1 capture input B pin
	CCP1B_O	O	CCP1 PWM output B pin
	RXD1	I	UART1 data input pin
	TXD1	O	UART1 data output pin
	PGA123_O	AO	PGA123 output channel

Pin number	Pin name	Pin type	Description
	DAC_O	AO	DAC voltage output channel
33	P54	I/O	GPIO is configured for input, output, pull-up, pull-down, and other functions through registers.
	C0P3	AI	ACMP0 positive input channel3
	RXD1	I	UART1 data input pin
	TXD1	O	UART1 data output pin
	SCL	I/O	I2C clock input/output pin
34	P55	I/O	GPIO is configured for input, output, pull-up, pull-down, and other functions through registers.
	C0N	AI	ACMP1 negative input channel
	BKIN	I	EPWM external brake signal input
	SDA	I/O	I2C data input/output pin
	RXD1	I	UART1 data input pin
	TXD1	O	UART1 data output pin
35	P56	I/O	GPIO is configured for input, output, pull-up, pull-down, and other functions through registers.
	AN5	AI	ADC channel 5 input
	CCP1A_I	I	CCP1 capture input A pin
	CCP1A_O	O	CCP1 PWM output A pin
	C0P2	AI	ACMP0 positive input channel2
	HALL_IN2	I	HALL input channel 2
36	P57	I/O	GPIO is configured for input, output, pull-up, pull-down, and other functions through registers.
	AN6	AI	ADC channel 6 input
	CCP1B_I	I	CCP1 capture input B pin
	CCP1B_O	O	CCP1 PWM output B pin
	C0P1	AI	ACMP0 positive input channel1
	HALL_IN1	I	HALL input channel 1
37	P00	I/O	GPIO is configured for input, output, pull-up, pull-down, and other functions through registers.
	AN7	AI	ADC channel 7 input
	C0P0	AI	ACMP0 positive input channel0
	HALL_IN0	I	HALL input channel 0
	ADC_TRIG	O	ADC module trigger signal output pin
	CCP0A_I	I	CCP0 capture input A pin
	CCP0A_O	O	CCP0 PWM output A pin
	RXD0	I	UART0 data input pin
	TXD0	O	UART0 data output pin
38	P01	I/O	GPIO is configured for input, output, pull-up, pull-down, and other functions through registers.
	NRST	I	External reset pin
	ADC_TRIG	O	ADC module trigger signal output pin

Pin number	Pin name	Pin type	Description
	CCP0B_I	I	CCP0 capture input B pin
	CCP0B_O	O	CCP0 PWM output B pin
	RXD0	I	UART0 data input pin
	TXD0	O	UART0 data output pin
39	VDD	P	Power supply
40	VSS	P	Ground

Alternate caution: INTP0, INTP1, INTP2, INTP3, TI00, TI01, TI02, TI03 can be mapped to any GPIO input. INTPn (n=0~3) is the external interrupt n input pin, and TI0n (n=0~3) is the input channel n of the universal timer unit 0.

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The symbols in the table below are described as follows:

Pin name	Symbol description
I/O	Digital input/output
I	Digital input
O	Digital output
AI	Analog input
AO	Analog output
P	Power or ground

Pin number	Pin name	Pin type	Description
3	P02	I/O	GPIO is configured for input, output, pull-up, pull-down, and other functions through registers.
	SWDDAT	I/O	SWD data port
	CCP1A_I	I	CCP1 capture input A pin
	CCP1A_O	O	CCP1 PWM output A pin
4	P03	I/O	GPIO is configured for input, output, pull-up, pull-down, and other functions through registers.
	SWDCLK	I	SWD clock port
	ADC_TRIG	O	ADC module trigger signal output pin
	CCP1B_I	I	CCP1 capture input B pin
	CCP1B_O	O	CCP1 PWM output B pin
5	P04	I/O	GPIO is configured for input, output, pull-up, pull-down, and other functions through registers.
	AN8	AI	ADC channel 8 input
	CCP1A_I	I	CCP1 capture input A pin
	CCP1A_O	O	CCP1 PWM output A pin
	OSCOUT	O	External crystal oscillator output port
	C0_O	O	ACMP0 output channel
	SCL	I/O	I2C clock input/output pin
6	P05	I/O	GPIO is configured for input, output, pull-up, pull-down, and other functions through registers.
	AN9	AI	ADC channel 9 input
	OSCIN	I	External crystal oscillator input port
	CCP1B_I	I	CCP1 capture input B pin
	CCP1B_O	O	CCP1 PWM output B pin
	SDA	I/O	I2C data input/output pin
7	P06	I/O	GPIO is configured for input, output, pull-up, pull-down, and other functions through registers.
	AN10	AI	ADC channel 10 input
	CCP0A_I	I	CCP0 capture input A pin

Pin number	Pin name	Pin type	Description
	CCP0A_O	O	CCP0 PWM output A pin
	NSS	I/O	SPI chip select pin
	SCL	I/O	I2C clock input/output pin
8	P07	I/O	GPIO is configured for input, output, pull-up, pull-down, and other functions through registers.
	AN11	AI	ADC channel 11 input
	CCP0B_I	I	CCP0 capture input B pin
	CCP0B_O	O	CCP0 PWM output B pin
	SCLK	I/O	SPI clock input/output pin
	SDA	I/O	I2C data input/output pin
9	P10	I/O	GPIO is configured for input, output, pull-up, pull-down, and other functions through registers.
	ADET	I	ADC external trigger signal input channel
	MOSI	I/O	SPI master output/slave input pin
10	P11	I/O	GPIO is configured for input, output, pull-up, pull-down, and other functions through registers.
	AN12	AI	ADC channel 12 input
	CCP1A_I	I	CCP1 capture input A pin
	CCP1A_O	O	CCP1 PWM output A pin
	C0_O	O	ACMP0 output channel
	MISO	I/O	SPI master input/slave output pin
11	P12	I/O	GPIO is configured for input, output, pull-up, pull-down, and other functions through registers.
	AN13	AI	ADC channel 13 input
	CCP1B_I	I	CCP1 capture input B pin
	CCP1B_O	O	CCP1 PWM output B pin
	DAC_O	AO	DAC output channel
12	P13	I/O	GPIO is configured for input, output, pull-up, pull-down, and other functions through registers.
	AN14	AI	ADC channel 14 input
	BKIN	I	EPWM external brake signal input
13	P20	I/O	GPIO is configured for input, output, pull-up, pull-down, and other functions through registers.
	AN16	AI	ADC channel 16 input
	C1P0	AI	ACMP1 positive input channel 0
	HALL_IN0	I	HALL input channel 0
14	P21	I/O	GPIO is configured for input, output, pull-up, pull-down, and other functions through registers.
	AN17	AI	ADC channel 17 input
	C1P1	AI	ACMP1 positive input channel 1
	ADC_TRIG	O	ADC module trigger signal output pin
	HALL_IN1	I	HALL input channel 1

Pin number	Pin name	Pin type	Description
15	P22	I/O	GPIO is configured for input, output, pull-up, pull-down, and other functions through registers.
	AN18	AI	ADC channel 18 input
	C1P2	AI	ACMP1 positive input channel 2
	ADC_TRIG	O	ADC module trigger signal output pin
	HALL_IN2	I	HALL input channel 2
16	P23	I/O	GPIO is configured for input, output, pull-up, pull-down, and other functions through registers.
	C1P3	AI	ACMP1 positive input channel 3
	C1_O	O	ACMP1 output channel
	BKIN	I	EPWM external brake signal input
	CCP0B_I	I	CCP0 capture input B pin
	CCP0B_O	O	CCP0 PWM output B pin
	RXD1	I	UART1 data input pin
	TXD1	O	UART1 data output pin
17	P24	I/O	GPIO is configured for input, output, pull-up, pull-down, and other functions through registers.
	AN19	AI	ADC channel 19 input
	C1N	AI	ACMP1 negative input channel
	CCP0A_I	I	CCP0 capture input A pin
	CCP0A_O	O	CCP0 PWM output A pin
	ADC_TRIG	O	ADC module trigger signal output pin
	RXD1	I	UART1 data input pin
	TXD1	O	UART1 data output pin
18	P25	I/O	GPIO is configured for input, output, pull-up, pull-down, and other functions through registers.
	CCP1A_I	I	CCP1 capture input A pin
	CCP1A_O	O	CCP1 PWM output A pin
	RXD1	I	UART1 data input pin
	TXD1	O	UART1 data output pin
	C1_O	O	ACMP1 output channel
19	P30	I/O	GPIO is configured for input, output, pull-up, pull-down, and other functions through registers.
	PGA3_P	AI	PGA3 positive input channel
20	P31	I/O	GPIO is configured for input, output, pull-up, pull-down, and other functions through registers.
	PGA3_N	AI	PGA3 negative input channel
21	P32	I/O	GPIO is configured for input, output, pull-up, pull-down, and other functions through registers.
	PGA2_P	AI	PGA2 positive input channel
22	P33	I/O	GPIO is configured for input, output, pull-up, pull-down, and other functions through registers.

Pin number	Pin name	Pin type	Description
	PGA2_N	AI	PGA2 negative input channel
37	P46	I/O	GPIO is configured for input, output, pull-up, pull-down, and other functions through registers.
	PGA1_P	AI	PGA1 positive input channel
38	P47	I/O	GPIO is configured for input, output, pull-up, pull-down, and other functions through registers.
	PGA1_N	AI	PGA1 negative input channel
39	P50	I/O	GPIO is configured for input, output, pull-up, pull-down, and other functions through registers.
	PGA0_P	AI	PGA0 positive input channel
40	P51	I/O	GPIO is configured for input, output, pull-up, pull-down, and other functions through registers.
	PGA0_N	AI	PGA0 negative input channel
41	P52	I/O	GPIO is configured for input, output, pull-up, pull-down, and other functions through registers.
	AN21	AI	ADC channel 21 input
	CCP0B_I	I	CCP0 capture input B pin
	CCP0B_O	O	CCP0 PWM output B pin
	PGA0_O	AO	PGA0 output channel
42	P53	I/O	GPIO is configured for input, output, pull-up, pull-down, and other functions through registers.
	AN22	AI	ADC channel 22 input
	CCP1B_I	I	CCP1 capture input B pin
	CCP1B_O	O	CCP1 PWM output B pin
	RXD1	I	UART1 data input pin
	TXD1	O	UART1 data output pin
	PGA123_O	AO	PGA123 output channel
	DAC_O	AO	DAC voltage output channel
43	P54	I/O	GPIO is configured for input, output, pull-up, pull-down, and other functions through registers.
	C0P3	AI	ACMP0 positive input channel3
	RXD1	I	UART1 data input pin
	TXD1	O	UART1 data output pin
	SCL	I/O	I2C clock input/output pin
44	P55	I/O	GPIO is configured for input, output, pull-up, pull-down, and other functions through registers.
	C0N	AI	ACMP1 negative input channel
	BKIN	I	EPWM external brake signal input
	SDA	I/O	I2C data input/output pin
	RXD1	I	UART1 data input pin
	TXD1	O	UART1 data output pin
45	P56	I/O	GPIO is configured for input, output, pull-up, pull-down, and other

Pin number	Pin name	Pin type	Description
			functions through registers.
	AN5	AI	ADC channel 5 input
	CCP1A_I	I	CCP1 capture input A pin
	CCP1A_O	O	CCP1 PWM output A pin
	C0P2	AI	ACMP0 positive input channel2
	HALL_IN2	I	HALL input channel 2
46	P57	I/O	GPIO is configured for input, output, pull-up, pull-down, and other functions through registers.
	AN6	AI	ADC channel 6 input
	CCP1B_I	I	CCP1 capture input B pin
	CCP1B_O	O	CCP1 PWM output B pin
	C0P1	AI	ACMP0 positive input channel1
	HALL_IN1	I	HALL input channel 1
47	P00	I/O	GPIO is configured for input, output, pull-up, pull-down, and other functions through registers.
	AN7	AI	ADC channel 7 input
	C0P0	AI	ACMP0 positive input channel0
	HALL_IN0	I	HALL input channel 0
	ADC_TRIG	O	ADC module trigger signal output pin
	CCP0A_I	I	CCP0 capture input A pin
	CCP0A_O	O	CCP0 PWM output A pin
	RXD0	I	UART0 data input pin
	TXD0	O	UART0 data output pin
48	P01	I/O	GPIO is configured for input, output, pull-up, pull-down, and other functions through registers.
	NRST	I	External reset pin
	ADC_TRIG	O	ADC module trigger signal output pin
	CCP0B_I	I	CCP0 capture input B pin
	CCP0B_O	O	CCP0 PWM output B pin
	RXD0	I	UART0 data input pin
	TXD0	O	UART0 data output pin
1	VDD	P	Power supply
2	VSS	P	Ground
23	PGND	P	Internal pre-driver ground pin
24	GVDD	P	Internal pre-driver power supply pin
25	GL3	O	Phase 3 low-side gate driver output pin
26	GL2	O	Phase 2 low-side gate driver output pin
27	GL1	O	Phase 1 low-side gate driver output pin
28	GHS3	P	Phase 3 high-side floating pin
29	GH3	O	Phase 3 high-side gate driver output pin
30	BOST3	P	Phase 3 high-side bootstrap power supply pin
31	GHS2	P	Phase 2 high-side floating pin

Pin number	Pin name	Pin type	Description
32	GH2	O	Phase 2 high-side gate driver output pin
33	BOST2	P	Phase 2 high-side bootstrap power supply pin
34	GHS1	P	Phase 1 high-side floating pin
35	GH1	O	Phase 1 high-side gate driver output pin
36	BOST1	P	Phase 1 high-side bootstrap power supply pin

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The symbols in the table below are described as follows:

Pin name	Symbol description
I/O	Digital input/output
I	Digital input
O	Digital output
AI	Analog input
AO	Analog output
P	Power or ground

Pin number	Pin name	Pin type	Description
48	P02	I/O	GPIO is configured for input, output, pull-up, pull-down, and other functions through registers.
	SWDDAT	I/O	SWD data port
	CCP1A_I	I	CCP1 capture input A pin
	CCP1A_O	O	CCP1 PWM output A pin
1	P03	I/O	GPIO is configured for input, output, pull-up, pull-down, and other functions through registers.
	SWDCLK	I	SWD clock port
	ADC_TRIG	O	ADC module trigger signal output pin
	CCP1B_I	I	CCP1 capture input B pin
	CCP1B_O	O	CCP1 PWM output B pin
2	P04	I/O	GPIO is configured for input, output, pull-up, pull-down, and other functions through registers.
	AN8	AI	ADC channel 8 input
	CCP1A_I	I	CCP1 capture input A pin
	CCP1A_O	O	CCP1 PWM output A pin
	OSCOUT	O	External crystal oscillator output port
	C0_O	O	ACMP0 output channel
	SCL	I/O	I2C clock input/output pin
3	P05	I/O	GPIO is configured for input, output, pull-up, pull-down, and other functions through registers.
	AN9	AI	ADC channel 9 input
	OSCIN	I	External crystal oscillator input port
	CCP1B_I	I	CCP1 capture input B pin
	CCP1B_O	O	CCP1 PWM output B pin
	SDA	I/O	I2C data input/output pin
4	P06	I/O	GPIO is configured for input, output, pull-up, pull-down, and other functions through registers.
	AN10	AI	ADC channel 10 input
	CCP0A_I	I	CCP0 capture input A pin

Pin number	Pin name	Pin type	Description
	CCP0A_O	O	CCP0 PWM output A pin
	NSS	I/O	SPI chip select pin
	SCL	I/O	I2C clock input/output pin
5	P07	I/O	GPIO is configured for input, output, pull-up, pull-down, and other functions through registers.
	AN11	AI	ADC channel 11 input
	CCP0B_I	I	CCP0 capture input B pin
	CCP0B_O	O	CCP0 PWM output B pin
	SCLK	I/O	SPI clock input/output pin
	SDA	I/O	I2C data input/output pin
6	P20	I/O	GPIO is configured for input, output, pull-up, pull-down, and other functions through registers.
	AN16	AI	ADC channel 16 input
	C1P0	AI	ACMP1 positive input channel 0
	HALL_IN0	I	HALL input channel 0
7	P21	I/O	GPIO is configured for input, output, pull-up, pull-down, and other functions through registers.
	AN17	AI	ADC channel 17 input
	C1P1	AI	ACMP1 positive input channel 1
	ADC_TRIG	O	ADC module trigger signal output pin
	HALL_IN1	I	HALL input channel 1
8	P22	I/O	GPIO is configured for input, output, pull-up, pull-down, and other functions through registers.
	AN18	AI	ADC channel 18 input
	C1P2	AI	ACMP1 positive input channel 2
	ADC_TRIG	O	ADC module trigger signal output pin
	HALL_IN2	I	HALL input channel 2
9	P23	I/O	GPIO is configured for input, output, pull-up, pull-down, and other functions through registers.
	C1P3	AI	ACMP1 positive input channel 3
	C1_O	O	ACMP1 output channel
	BKIN	I	EPWM external brake signal input
	CCP0B_I	I	CCP0 capture input B pin
	CCP0B_O	O	CCP0 PWM output B pin
	RXD1	I	UART1 data input pin
	TXD1	O	UART1 data output pin
10	P24	I/O	GPIO is configured for input, output, pull-up, pull-down, and other functions through registers.
	AN19	AI	ADC channel 19 input
	C1N	AI	ACMP1 negative input channel
	CCP0A_I	I	CCP0 capture input A pin
	CCP0A_O	O	CCP0 PWM output A pin

Pin number	Pin name	Pin type	Description
	ADC_TRIG	O	ADC module trigger signal output pin
	RXD1	I	UART1 data input pin
	TXD1	O	UART1 data output pin
11	P30	I/O	GPIO is configured for input, output, pull-up, pull-down, and other functions through registers.
	PGA3_P	AI	PGA3 positive input channel
12	P31	I/O	GPIO is configured for input, output, pull-up, pull-down, and other functions through registers.
	PGA3_N	AI	PGA3 negative input channel
13	P32	I/O	GPIO is configured for input, output, pull-up, pull-down, and other functions through registers.
	PGA2_P	AI	PGA2 positive input channel
34	P46	I/O	GPIO is configured for input, output, pull-up, pull-down, and other functions through registers.
	PGA1_P	AI	PGA1 positive input channel
35	P47	I/O	GPIO is configured for input, output, pull-up, pull-down, and other functions through registers.
	PGA1_N	AI	PGA1 negative input channel
36	P50	I/O	GPIO is configured for input, output, pull-up, pull-down, and other functions through registers.
	PGA0_P	AI	PGA0 positive input channel
37	P51	I/O	GPIO is configured for input, output, pull-up, pull-down, and other functions through registers.
	PGA0_N	AI	PGA0 negative input channel
38	P52	I/O	GPIO is configured for input, output, pull-up, pull-down, and other functions through registers.
	AN21	AI	ADC channel 21 input
	CCP0B_I	I	CCP0 capture input B pin
	CCP0B_O	O	CCP0 PWM output B pin
	PGA0_O	AO	PGA0 output channel
39	P53	I/O	GPIO is configured for input, output, pull-up, pull-down, and other functions through registers.
	AN22	AI	ADC channel 22 input
	CCP1B_I	I	CCP1 capture input B pin
	CCP1B_O	O	CCP1 PWM output B pin
	RXD1	I	UART1 data input pin
	TXD1	O	UART1 data output pin
	PGA123_O	AO	PGA123 output channel
	DAC_O	AO	DAC voltage output channel
40	P54	I/O	GPIO is configured for input, output, pull-up, pull-down, and other functions through registers.
	C0P3	AI	ACMP0 positive input channel3

Pin number	Pin name	Pin type	Description
	RXD1	I	UART1 data input pin
	TXD1	O	UART1 data output pin
	SCL	I/O	I2C clock input/output pin
41	P55	I/O	GPIO is configured for input, output, pull-up, pull-down, and other functions through registers.
	C0N	AI	ACMP1 negative input channel
	BKIN	I	EPWM external brake signal input
	SDA	I/O	I2C data input/output pin
	RXD1	I	UART1 data input pin
	TXD1	O	UART1 data output pin
42	P56	I/O	GPIO is configured for input, output, pull-up, pull-down, and other functions through registers.
	AN5	AI	ADC channel 5 input
	CCP1A_I	I	CCP1 capture input A pin
	CCP1A_O	O	CCP1 PWM output A pin
	C0P2	AI	ACMP0 positive input channel2
	HALL_IN2	I	HALL input channel 2
43	P57	I/O	GPIO is configured for input, output, pull-up, pull-down, and other functions through registers.
	AN6	AI	ADC channel 6 input
	CCP1B_I	I	CCP1 capture input B pin
	CCP1B_O	O	CCP1 PWM output B pin
	C0P1	AI	ACMP0 positive input channel1
	HALL_IN1	I	HALL input channel 1
44	P00	I/O	GPIO is configured for input, output, pull-up, pull-down, and other functions through registers.
	AN7	AI	ADC channel 7 input
	C0P0	AI	ACMP0 positive input channel0
	HALL_IN0	I	HALL input channel 0
	ADC_TRIG	O	ADC module trigger signal output pin
	CCP0A_I	I	CCP0 capture input A pin
	CCP0A_O	O	CCP0 PWM output A pin
	RXD0	I	UART0 data input pin
	TXD0	O	UART0 data output pin
45	P01	I/O	GPIO is configured for input, output, pull-up, pull-down, and other functions through registers.
	NRST	I	External reset pin
	ADC_TRIG	O	ADC module trigger signal output pin
	CCP0B_I	I	CCP0 capture input B pin
	CCP0B_O	O	CCP0 PWM output B pin
	RXD0	I	UART0 data input pin
	TXD0	O	UART0 data output pin

Pin number	Pin name	Pin type	Description
46	VDD	P	Power supply
47	VSS	P	Ground
20	GVDD	P	Internal pre-drive power pin (LDO12V output is internally connected to the pre-drive power supply)
21	PGND	P	Internal pre-drive ground pin
22	GL3	O	Phase 3 low-side gate driver output pin
23	GL2	O	Phase 2 low-side gate driver output pin
24	GL1	O	Phase 1 low-side gate driver output pin
25	GHS3	P	Phase 3 high-side floating pin
26	GH3	O	Phase 3 high-side gate driver output pin
27	BOST3	P	Phase 3 high-side bootstrap power supply pin
28	GHS2	P	Phase 2 high-side floating pin
29	GH2	O	Phase 2 high-side gate driver output pin
30	BOST2	P	Phase 2 high-side bootstrap power supply pin
31	GHS1	P	Phase 1 high-side floating pin
32	GH1	O	Phase 1 high-side gate driver output pin
33	BOST1	P	Phase 1 high-side bootstrap power supply pin
14	SE	I	Power-on self-test
15	KEY	I	12V\5V LDO enable signal
16	EN	I	MCU enable signal controller
17	VOUT	O	Power supply voltage divider output pin
18	VBAT	P	Chip power supply pin
19	VERG5V	O	5V regulated output pin

4.5 Pin Function List

Function name	Input	Alternate function PmnCFG			
		0	1	2	3
P00	HALL_IN0/RXD0/CCP0A_I		TXD0	CCP0A_O	ADC_TRIG
P01	NRST/RXD0/CCP0B_I		TXD0	CCP0B_O	ADC_TRIG
P02	CCP1A_I		-	CCP1A_O	-
P03	CCP1B_I		-	CCP1B_O	ADC_TRIG
P04	CCP1A_I		C0_O	CCP1A_O	SCL
P05	CCP1B_I		-	CCP1B_O	SDA
P06	CCP0A_I		NSS	CCP0A_O	SCL
P07	CCP0B_I		SCLK	CCP0B_O	SDA
P10	ADET		MOSI	-	-
P11	CCP1A_I		MISO	CCP1A_O	C0_O
P12	CCP1B_I		-	CCP1B_O	-
P13	BKIN	--	-	-	-
P14	-		MISO	PCUBZ0	SCL
P15	RXD0		MOSI	TXD0	SDA
P16	BKIN/RXD0		SCLK	TXD0	-
P17	-		NSS	-	ADC_TRIG
P20	HALL_IN0		-	-	-
P21	HALL_IN1		-	-	ADC_TRIG
P22	HALL_IN2		-	-	ADC_TRIG
P23	BKIN/RXD1/CCP0B_I		TXD1	CCP0B_O	C1_O
P24	RXD1/CCP0A_I		TXD1	CCP0A_O	ADC_TRIG
P25	RXD1/CCP1A_I		TXD1	CCP1A_O	C1_O
P30	-		-	-	-
P31	-	-	-	-	-
P32	-		-	-	-
P33	-		-	-	-
P34	RXD0		TXD0	-	SDA
P35	RXD0		TXD0	-	SCL
P36	-		EPWM0	-	-
P37	-		EPWM1	-	-
P40	-		EPWM2	-	-
P41	-		EPWM3	-	-
P42	-		EPWM4	-	-
P43	-		EPWM5	-	-
P44	-		EPWM6	-	-
P45	-		EPWM7	-	-
P46	-		-	-	-
P47	-		-	-	-

P50	-		-	-	-
P51	-		-	-	-
P52	CCP0B_I		-	CCP0B_O	-
P53	RXD1/ CCP1B_I		TXD1	CCP1B_O	-
P54	RXD1		TXD1	-	SCL
P55	BKIN/RXD1		TXD1	-	SDA
P56	HALL_IN2/CCP1A_I		-	CCP1A_O	
P57	HALL_IN1/ CCP1B_I		-	CCP1B_O	

Remarks:

1. The I/O alternate function of this product requires the user to configure PMC, PM, and other registers separately.
2. When the IIC function is selected, the open-drain function is automatically enabled.
3. For the alternate function that can be used both as input and output, the input channel is automatically enabled once the PmnCFG is configured.
4. For the port input alternate function, the corresponding PSxx_CFG should be set to select the I/O pin.
5. INTP0, INTP1, INTP2, INTP3, TI00, TI01, TI02, TI03 can be mapped to any GPIO input.

The analog and special function pins are listed below:

Pin	Analog			Special function pin
	ADC	ACMP	PGA	
P00	AN7	C0P0	-	-
P01	-	-	-	NRST
P02	-	-	-	SWDDAT
P03	-	-	-	SWDCLK
P04	AN8	-	-	OSCOUT
P05	AN9	-	-	OSCIN
P06	AN10	-	-	-
P07	AN11	-	-	-
P10	-	-	--	-
P11	AN12	-	-	-
P12	AN13	-	-	DAC_O
P13	AN14	-	-	-
P14	AN15	-	-	-
P15	-	-	-	-
P16	-	-	-	-
P17	-	-	-	-
P20	AN16	C1P0	-	-
P21	AN17	C1P1	-	-
P22	AN18	C1P2	-	-
P23	-	C1P3	-	-
P24	AN19	CIN	-	-
P25	-	-	-	-
P30	-	-	PGA3_P	-
P31	-	-	PGA3_N	-
P32	-	-	PGA2_P	-
P33	-	-	PGA2_N	-
P34	AN20	-	-	-
P35	-	-	-	-
P36	-	-	-	-
P37	-	-	-	-
P40	-	-	-	-
P41	-	-	-	-
P42	-	-	-	-
P43	-	-	-	-
P44		-	-	-
P45	-	-	-	-
P46	-	-	PGA1_P	-
P47	-	-	PGA1_N	-
P50	-	-	PGA0_P	-
P51	-	-	PGA0_N	-

P52	AN21	-	PGA0_O	-
P53	AN22	-	PGA123_O	DAC_O
P54	-	C0P3	-	-
P55	-	C0N	-	-
P56	AN5	C0P2	-	-
P57	AN6	C0P1	-	-

5. Function Summary

5.1 ARM® Cortex®-M0+ Core

The ARM Cortex-M0+ processor is a next-generation product in the ARM processor family, designed specifically for embedded systems. It provides a low-cost platform aimed at meeting the demands of microcontrollers with fewer pins and low power consumption, while offering excellent computational performance and advanced system response to interrupts.

The Cortex-M0+ processor is a 32-bit microcontroller that delivers outstanding code efficiency and high-performance expectations of the ARM core, differentiating it from 8-bit and 16-bit devices with the same memory size. The Cortex-M0+ processor features 32 address lines, supporting memory space up to 4GB.

The CMS32M67xx series uses the embedded ARM core, ensuring compatibility with all ARM tools and software.

5.2 Memory

5.2.1 Flash Memory

The product features built-in programmable, erasable, and readable flash memory with the following capabilities:

- Program and data share a 128KB memory space.
- 1KB dedicated data Flash memory.
- Supports page erase operation, with each page size being 512 bytes.
- Supports byte/half-word programming.
- Supports CRC for the program area.

5.2.2 SRAM

The chip integrates two embedded SRAMs: SRAM0 (4KB) and SRAM1 (8KB).

5.3 Clock Generation and Start-Up

A clock generation circuit is a circuit that generates a clock to the CPU and peripheral hardware. There are two types of system clocks and clock oscillation circuits.

5.3.1 Main System Clock

- High-speed On-Chip Oscillator (High-speed OCO): 72MHz/64MHz, which can be divided into 36MHz/18MHz/9MHz/4.5MHz, or 32MHz/16MHz/8MHz/4MHz/2MHz.
- X1 Oscillator Clock Circuit: 4MHz to 8MHz.
- PLL Clock: Provides clock signals after frequency division from either X1 or the high-speed OCO, with a maximum output clock of 72MHz and a minimum output clock of 48MHz.
- Clock Output: The main system clock, with the output clock being less than 16MHz.

5.3.2 Low-Speed On-Chip Oscillator Clock

Low-speed On-Chip Oscillator (Low-speed OCO): 15KHz. The following peripheral hardware can operate using the low-speed on-chip oscillator clock:

- Watchdog Timer (WDT)
- LSITIMER Timer

5.4 Power Management

5.4.1 Power Supply Method

V_{DD}: External power supply, and voltage range is 1.8 to 5.5V.

5.4.2 Power-on Reset

The power-on-reset circuit (POR) has the following functions:

- An internal reset signal is generated when power is applied. If the supply voltage (V_{DD}) is greater than the detection voltage (V_{POR}), the reset is released. However, the reset state must be maintained by a voltage detection circuit or an external reset until the operating voltage range is reached.
- The power supply voltage (V_{DD}) is compared with the detection voltage (V_{POR}) and an internal reset signal is generated when $V_{DD} < V_{POR}$. However, when the power supply drops, it must be shifted to deep sleep mode or set to reset by voltage detection circuit or external reset before it is less than the operating voltage range. To restart operation, it must be confirmed that the power supply voltage has returned to the operating voltage range.

Remark: 1. VPOR: POR supply voltage rise detection voltage
VPDR: POR supply voltage fall detection voltage

5.4.3 Voltage Detection

The voltage detection circuit sets the operation mode and detection voltage (V_{LVDH}, V_{LVDL}, V_{LVD}) by means of option bytes. The voltage detection (LVD) circuit has the following functions:

- The internal reset or interrupt request signal is generated by comparing the power supply voltage (V_{DD}) with the detection voltage (V_{LVDH}, V_{LVDL}, V_{LVD}).
- The detection voltage of the supply voltage (V_{LVDH}, V_{LVDL}, V_{LVD}) can be selected via the option byte.
- Able to run in deep sleep mode.
- When the power supply rises, the reset state must be maintained by voltage detection circuitry or external reset before the operating voltage range is reached. When the power supply drops, it must be shifted to deep sleep mode or set to reset state by voltage detection circuit or external reset before it is less than the operating voltage range.
- The operating voltage range varies according to the setting of the user option byte.

5.5 Low-Power Consumption Modes

The product supports two low-power modes to achieve the best compromise between low power consumption, short start-up time, and available wake-up sources:

- Sleep Mode: Entered by executing the sleep instruction. In this mode, the CPU clock is stopped. However, if the high-speed on-chip oscillator or low-speed on-chip oscillator is still oscillating, the clocks will continue to oscillate. While this mode does not reduce the operating current to the extent of deep sleep mode, it is effective for situations where immediate processing is required via interrupt requests or for intermittent operation.
- Deep Sleep Mode: Entered by executing the deep sleep instruction. In this mode, the high-speed on-chip oscillator is stopped, and the entire system is powered down. This significantly reduces the chip's operating current. Deep sleep mode can be released via an interrupt request, allowing for intermittent operation.
- Partial Power-Down Deep Sleep Mode: Entered by executing the deep sleep instruction after the PMUKEY instruction has been configured to grant permission. In this mode, compared to deep sleep mode, some peripheral power supplies are turned off, further reducing the chip's operating current. Partial power-down deep sleep mode can also be released via interrupt requests, allowing for intermittent operation.

In all modes, except for partial power-down deep sleep mode, registers, flags, and data memory are retained as they were before entering the standby mode. The input/output port output latches and output buffers also maintain their state. However, releasing partial power-down deep sleep mode requires re-initializing peripheral modules and other functions.

5.6 Reset Function

This product has six methods to generate a reset signal:

- An external reset is triggered by a signal input through the RESETB pin.
- An internal reset is generated by the watchdog timer if a program failure is detected.
- An internal reset is triggered by the comparison of the power supply voltage and the detection voltage in the power-on reset circuit.
- An internal reset is generated by the comparison of the power supply voltage and the detection voltage in the voltage detection circuit (LVD).
- An internal reset is generated when the AIRCR.SYSRESETREQ bit in the system reset request register is set to 1.
- An internal reset is triggered by an illegal memory access.

The internal reset is the same as the external reset, and after generating the reset signal, program execution starts from the user-defined program start address.

5.7 Interrupt Function

The Cortex-M0+ processor is equipped with a Nested Vectored Interrupt Controller (NVIC), which supports up to 23 interrupt request (IRQ) inputs and 1 non-maskable interrupt (NMI) input. Additionally, the processor supports multiple internal exceptions.

This product handles 23 maskable interrupt requests (IRQ) and 1 non-maskable interrupt (NMI). For more details, please refer to the relevant section in the user manual.

5.8 Timers

5.8.1 SysTick Timer

This timer is specific to real-time operating systems, but can also be used as a standard decrement counter. It features a 24-bit decrement counter when the self-loading capacity counter reaches 0, and a maskable system interrupt is generated.

5.8.2 Watchdog Timer

The 1-channel Watchdog Timer (WDT) is a 17-bit timer that runs based on the clock set through the option byte. The Watchdog Timer operates with a low-speed on-chip oscillator clock (15kHz). It is used to detect program failures, and when a failure is detected, it generates an internal reset signal.

The following situations are considered as program failures:

- When the Watchdog Timer counter overflows.
- When data other than “ACH” is written to the WDTE register.
- When data is written to the WDTE register during the window close period.

5.8.3 Universal Timer Unit

This product includes a general-purpose timer unit with 1 module containing 4 channels, each being a 16-bit timer. Each 16-bit timer is referred to as a “channel”, and can be used either as an independent timer or combined with other channels to provide more advanced timer functionalities.

For detailed information about each function, please refer to the table below.

Independent channel operation function	Multi-channel linkage operation function	8-bit timer operation function
● Interval timer ● Square wave output ● External event counter ● Frequency divider ● Measurement of input pulse interval ● Measurement of high/low level width of input signal ● Delay counter	● Single trigger pulse output ● PWM output ● Multiple PWM output	● The 16-bit timer channels can be used as two 8-bit timer channels. (Only channels 1 and 3 can be used.)

5.8.4 Universal Timers (Timer0/1)

The product includes two programmable 32-bit/16-bit down counters, providing convenient timing and counting functions for users. Timer0-Timer1 have the following features:

- The counting clock can be selected with prescalers of 1, 16, or 256.
- Each timer has an independent prescaler.
- It supports three counting modes: single trigger, periodic counting, and continuous counting.
- Supports delayed loading of the initial count value.
- Supports generating interrupts when the counter decrements to zero.
- Supports waking up the chip from sleep mode.

5.8.5 12-Bit Interval Timer (LSITIMER)

This product features a built-in 12-bit interval timer, which can generate interrupts (INTIT) at a user-defined time interval. It can be used to wake up from sleep mode, deep sleep mode, and partial power-down mode.

5.9 Communication Modules

5.9.1 Universal Asynchronous Receiver/Transmitter (UARTn, n=0/1)

This product includes two full-duplex asynchronous communication interfaces, UART0 and UART1. The UART transceivers have the following features:

- Full-duplex, asynchronous communication.
- Data bit length can be set from 5 to 8 bits.
- Stop bit length can be set to 1 bit, 1.5 bits, or 2 bits.
- Parity bit can be set to odd, even, no parity, or fixed parity bit generation and detection.

5.9.2 Serial Peripheral Interface Controller (SSP/SPI)

This product includes a synchronous serial controller SSP/SPI that operates in full-duplex mode. The SSP/SPI controller has the following features:

- Compatible with Motorola's SPI, TI's 4-wire SSI, and NS's Microwire bus.
- Supports both master and slave modes.
- Configurable data bit length for transmission (4-bit to 16-bit).
- Configurable clock polarity and phase.
- Programmable clock rate control.
- MSB first for transmission/reception.
- An internal receive buffer and an internal transmit buffer.

5.9.3 Standard Serial Interface (IICA)

This product includes a two-wire bidirectional serial bus controller, I^2C. The I^2C controller has the following features:

- Standard I^2C-compatible bus interface.
- Supports both master and slave modes, with bidirectional data transfer between master and slave.
- Arbitration for simultaneous data transmission among multiple masters, preventing serial data corruption on the bus.
- The bus uses a serial synchronized clock, allowing devices to communicate at different transfer rates.
- Programmable clock for controlling various rates.
- Supports 7-bit slave address mode.

5.10Enhanced Peripherals

5.10.1 Division Operation Unit (DIV)

This product includes a 32-bit/32-bit hardware divider. The divider has the following features:

- Supports both signed and unsigned division operations.
- Both quotient and remainder are 32 bits wide.
- Division-by-zero flag indicator.
- Completes operations in 22 APB clock cycles.
- The operation is initiated by writing to the ALUB register.

5.10.2 Division and Square Root Operation Unit (DIVSQRT)

This product includes a 32-bit hardware divider and square root unit. The unit has the following features:

- Supports both signed and unsigned division and square root operations.
- Both quotient and remainder are 32 bits wide.
- Division-by-zero flag indicator.
- Completes operations in 22 APB clock cycles.
- The operation is initiated by writing to the ALUB register.

5.10.3 Capture/Compare/Pulse Width Modulation Module (CCP0/1)

This product includes two sets of CCP modules: CCP0 and CCP1, each corresponding to two channels: A and B. The CCP modules support PWM output, capture modes 0, 1, and 2, and interrupt functionality.

1) PWM output features:

- CCP0: Channels A and B share the same period register. CCP1: Channels A and B share another period register.
- The duty cycle of the A and B channels of CCP0/CCP1 can be set independently.
- The output duty cycles of CCP0/CCP1's A and B channels can be set independently.
- Up to 4 PWM outputs can be generated.
- 50% duty cycle square wave output is supported.
- Output polarity is selectable.

2) Capture mode 0 features:

- CCP0 can select either the A or B channel as an external capture input signal.
- CCP1 can select either the A or B channel as an external capture input signal.
- CCP0 has a 16-bit internal counter.
- CCP1 has a 32-bit internal counter.
- Four capture modes are available: software start counting with rising edge capture, software start counting with falling edge capture, rising edge count with falling edge capture, and falling edge count with rising edge capture.
- Capture condition triggered, counter stopped.

3) Capture mode 1 features:

- Only CCP1 has capture mode 1.
- Four capture channels, CAP0, CAP1, CAP2, and CAP3, each with a 4-bit control for selecting different inputs.
- Software capture mode triggered by writing to a register.
- Rising edge, falling edge, and double edge triggering of external signals can be selected for edge capture.
- Supports CCP1 capture triggering CCP0 counter loading enable.

4) Capture mode 2 features:

- Only CCP1 has capture mode 2; CCP0 can be freely configured.
- CAP1, CAP2, and CAP3 share the same capture channel, capturing the same signal.
- Each channel can independently select rising edge, falling edge, or both edges of the external signal as edge-triggered capture.
- After CCP1 capture is completed, automatic calculation of period and duty cycle data is available.

5) CCP module interrupts:

- Counter compare interrupt.
- Capture Mode 0 capture interrupt.
- Capture Mode 1 interrupts for CAP0, CAP1, CAP2, CAP3.
- Capture Mode 2 interrupts for CAP1, CAP2, CAP3.
- Counter overflow interrupt.

5.10.4 Enhanced PWM (EPWM)

The Enhanced PWM (EPWM) module supports 8 PWM generators, where the period and duty cycle can be set independently. EPWM has the following features:

- Single-mode (only supports edge-aligned) or Auto-reload mode.
- Supports four control modes: Independent, Complementary, Synchronized, and Grouped control.
- The counting clock can be selected with a prescaler of 1, 2, 4, 8, or 16.
- Supports two counting modes: Edge-aligned and Center-aligned.
- In center-aligned mode, both symmetrical counting and asymmetrical counting are supported.
- Each PWM channel has independent polarity control.
- Supports period, upward comparison, downward comparison, and zero-cross interrupt.
- Fault brake protection and recovery functions (software/hardware trigger and software/hardware recovery).
- ACMP0/1 outputs and ADC comparator outputs can trigger hardware brake protection.
- PWM edge, period points, zero-cross, and comparison points 0/1 can trigger ADC conversion start.
- For complementary PWM, a programmable dead-time generator is supported.

5.10.5 Enhanced DMA

This product integrates an Enhanced DMA (Direct Memory Access) controller, which enables data transfer between memories without using the CPU. The module has the following features:

- Data transfer length can be selected as 8-bit, 16-bit, or 32-bit.
- Supports initiating DMA through peripheral interrupt triggers, allowing data transfer.
- The source and target address space can be selected from the entire address range (when Flash is the target, it needs to be set to programming mode).
- Supports three transfer modes: normal transfer mode, repeat transfer mode, and chain transfer mode.

5.10.6 HALL Signal Processing Module

This series of products includes a HALL signal processing module, primarily designed to process input signals from sensors. The module features the following characteristics:

- Supports 3 channels of HALL sensor input signals.
- The 3 channels are independent of each other.
- Each channel includes two stages of filters.
- Supports HALL signal capture, recording the time of signal changes and triggering interrupts.
- Supports software-triggered interrupts for signal changes.
- Includes a 32-bit independent counter, which supports overflow interrupts.
- Supports real-time input signal and filtering result outputs.

5.11Analog Modules

5.11.1 Analog-to-Digital Converter (ADC)

This product includes a 12-bit, 27-channel fast successive approximation type Analog-to-Digital Converter (ADC), supporting both one-shot and continuous conversion modes. The module has the following features:

- Reference voltage options: VDD/4.2V/3.6V.
- Maximum sampling rate: 1.2 Msps.
- Supports up to 27 single-ended analog input channels.
- Supports two power modes: High-speed mode and Low-current mode.
- In high-speed mode, the time to complete a conversion is 52*T_{ADCK} (with a sampling time set to 13.5*T_{ADCK}).
- One-shot mode: Performs one A/D conversion on the specified channel.
- Continuous mode: Performs A/D conversions on all selected channels.
- Supports generating an interrupt when the conversion is completed.
- Includes a built-in AD conversion result comparator.
- The conversion result of each channel is stored in its corresponding data register.

5.11.2 Analog Comparators (ACMP0/1)

This product contains 2 analog comparators, ACMP0 and ACMP1, with the following features:

- Analog input voltage range: 0 to (V_{DD})V.
- Supports single-sided and dual-sided hysteresis functions.
- Supports selectable hysteresis voltage (10mV/20mV/60mV – typical values).
- The positive input of each comparator can be multiplexed to multiple channels.
- The negative input of each comparator can be selected from either a port input or an internal reference voltage.
- Output filter time is selectable: 0 to 512*Tsys.
- Comparator output polarity is selectable.
- Both the comparator output and event generation output can serve as brake trigger signals for enhanced PWM.
- Interrupt generation can be triggered by both event generation and the comparator output.
- Supports window function, with selectable window polarity.
- ACMP0/1 each have four EPWM window channels available for selection.

5.11.3 Programmable Gain Amplifiers (PGA0/1/2/3)

This product includes 4 programmable gain amplifiers (PGAs): PGA0, PGA1, PGA2, PGA3, each with the following features:

- Adjustable gain: 1X/2X/2.5X/5X/7.5X/10X/15X.
- PGA0 reference voltage: BGR(0.8V) or $V_{REF}/2$
- PGA1/2/3 reference voltage: $V_{REF}/2$.
- Selectable output mode.

5.11.4 Digital-to-Analog Converter (DAC)

This product contains a Digital-to-Analog Converter (DAC) with the following features:

- Selectable analog input voltage: V_{DD}/4.2V/3.6V.
- Selectable multiple output voltage levels.

5.11.5 Temperature Sensor

This product is equipped with an on-chip temperature sensor that can measure and monitor the core temperature of the product, ensuring its reliable operation.

5.12Safety Features

5.12.1 Flash Memory CRC Operation (High-Speed CRC, Universal CRC)

The CRC operation is used to detect data errors in flash memory. Depending on the application and usage conditions, two types of CRCs can be used:

- High-speed CRC: During the initialization process, it can stop the CPU operation and quickly check the entire code flash area.
- Universal CRC: Can be used for multiple-purpose checks while the CPU is running, without being limited to the code flash area.

Both CRC modules use the CRC-16-CCITT polynomial "$X^{16}+X^{12}+X^5+1$" for checksum generation.

5.12.2 SFR Guard Function

Some of the SFRs of the key function modules are protected, and the write operation is invalid in the protected state and can be read normally.

5.12.3 Illegal Memory Access Detection Function

It detects illegal access to an illegal memory area (an area with no memory or an area with restricted access).

5.12.4 Frequency Detection Function

It can self detect the CPU/peripheral hardware clock frequency by the timer unit.

5.12.5 A/D Test Function

Performs A/D conversion on the following signals to confirm proper operation of the A/D converter: positive reference voltage, negative reference voltage, analog input channels, output voltage from the temperature sensor, internal reference voltage

5.12.6 I/O Port Digital Output Signal Level Detection

When an input/output pin is in output mode, it is possible to read the output signal level of the pin.

5.12.7 Unique Product Identifier Register

A 128-bit unique product identifier is provided for each microcontroller. This identifier is guaranteed to be unique in all cases and cannot be modified by the user.

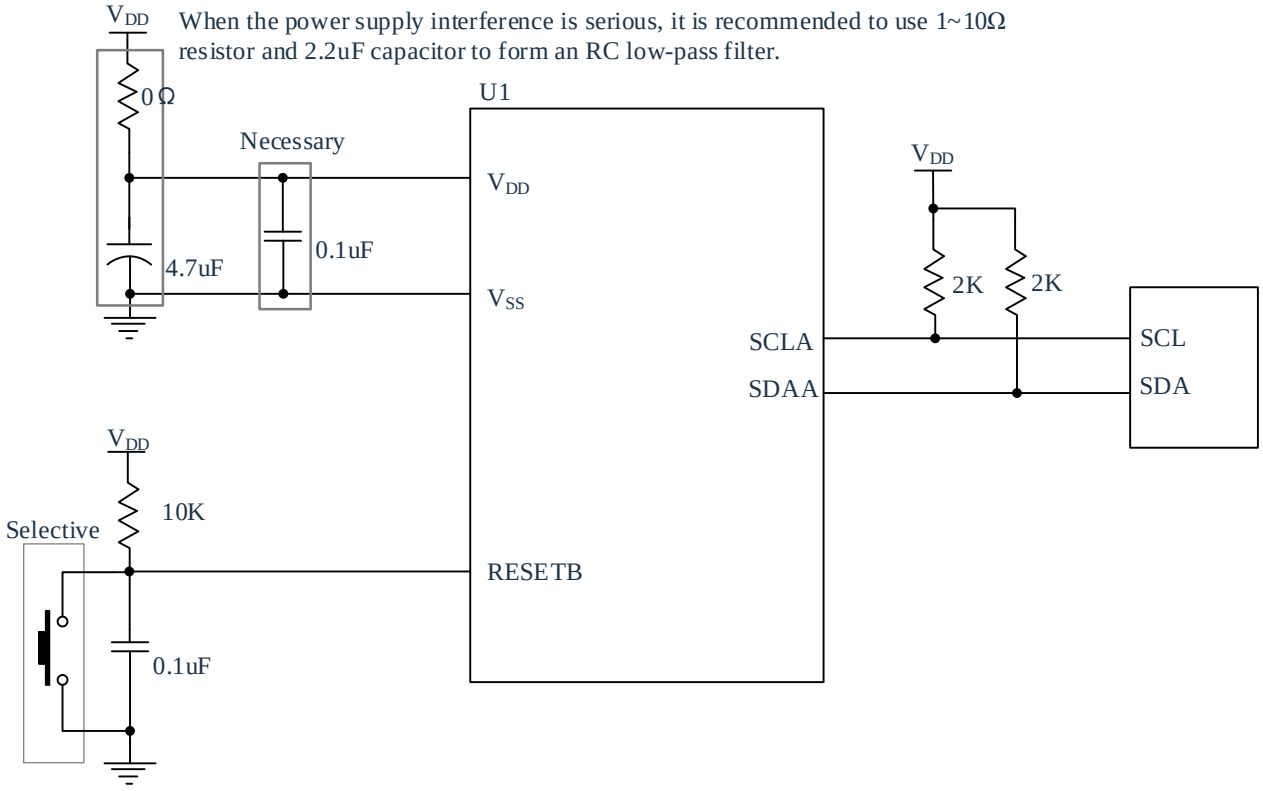
5.13Two-Wire Serial Debug Port (SW-DP)

The ARM SW-DP interface allows connection to the microcontroller via a serial wire debugger tool.

6. Electrical Characteristics

6.1 Typical Application Peripheral Circuit

The device connection reference for the peripheral circuit of a typical MCU application is shown as follows.



6.2 Absolute Maximum Voltage Ratings

(T_A= -40~105℃)

Item	Symbol	Condition	Rating	Unit
Supply voltage	V_{DD}	-	-0.5~6.5	V
Input voltage	V_I	P00~P07, P10~P17, P20~P25, P30~P37, P40~P47, P50~P57	-0.3~V_{DD}+0.3[Note 1]	V
Output voltage	V_O	P00~P07, P10~P17, P20~P25, P30~P37, P40~P47, P50~P57	-0.3~V_{DD}+0.3[Note 1]	V
Analog input voltage	V_{AI}	AN0~AN23	-0.3~V_{DD}+0.3	V

Note 1: No more than 6.5V.

Caution: Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

Remarks:

1. Unless otherwise specified, the characteristics of multiplexed pins are the same as those of port pins.
2. Use V_{SS} as the reference voltage.
3. Low temperature specification values are guaranteed by design, and low temperature conditions are not tested in mass production.

6.3 Absolute Maximum Current Ratings

(T_A= -40~105℃)

Item	Symbol	Condition		Rating	Unit
Output current, high	I_{OH}	Per pin	P00~P07, P10~P17, P20~P25, P30~P37, P40~P47, P50~P57	-10	mA
		Total of all pins	P10~P17, P20~P25, P30~P37, P40~P47	-50	mA
			P00~P07, P50~P57	-70	mA
Output current, low	I_{OL}	Per pin	P00~P07, P10~P17, P20~P25, P30~P37, P40~P47, P50~P57	20	mA
		Total of all pins	P10~P17, P20~P25, P30~P37, P40~P47	60	mA
			P00~P07, P50~P57	70	mA
Operating ambient temperature	T_A	In normal operation mode		-40~105	℃
		In flash memory programming mode			
Storage temperature	T_{stg}	-		-65~150	℃

Caution: Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

Remarks:

1. Unless otherwise specified, the characteristics of multiplexed pins are the same as those of port pins.
2. Low-temperature specification values are guaranteed by the design, and are not tested in mass production.

6.4 Oscillation Circuit Characteristics

6.4.1 X1 Characteristics

（TA= –40～105℃、1.8V≤VDD≤5.5V、VSS=0V）

Item	Resonator	Condition	Min.	Typ.	Max.	Unit
X1 clock oscillation frequency (fx)	Ceramic resonator / Crystal resonator	C = 5~20pf	4.0	-	16.0	MHz

Note 1:It only indicates the allowable frequency range of the oscillation circuit. For the instruction execution time, please refer to the AC characteristic.

Note 2: Please entrust the resonator manufacturer to conduct an assessment after the installation of the circuit and use it after confirming the oscillation characteristics.

6.4.2 On-Chip Oscillator Characteristics

(T_A= -40~105℃, 1.8V≤V_{DD}≤5.5V, V_{SS}=0V)

Resonator	Condition	Min.	Typ.	Max.	Unit
High-speed on-chip oscillator clock frequency (F_{IH})Note 1,2	-	1.0	-	72.0	MHz
High-speed on-chip oscillator clock frequency accuracy	T_A= 0~85℃	-1.5	-	+1.5	%
	T_A= -40~105℃	-2	-	+2	%
Low-speed on-chip oscillator clock frequency (F_{IL})	-	13.5	15	16.5	KHz

Note 1: The frequency of the high-speed on-chip oscillator is selected via the option byte.

Note 2: This indicates the oscillator characteristics only. Refer to AC Characteristics for instruction execution time.

Remark: Low-temperature specification values are guaranteed by the design, and are not tested in mass production.

6.5 DC Characteristics

6.5.1 Pin Characteristics

(T_A= -40~105℃, 1.8V≤V_{DD}≤5.5V, V_{SS}=0V)

Item	Symbol	Condition		Min.	Typ.	Max.	Unit
Output current, high Note 1	I_{OH}	Per pin for P00~P07, P10~P17, P20~P25, P30~P37, P40~P47, P50~P57	1.8V≤V_{DD}≤5.5V -40~105℃	-	-	-8.0 Note 2	mA
		Total of P10~P17, P20~P25, P30~P37, P40~P47 (When duty≤70% Note 3)	4.0V≤V_{DD}≤5.5V -40~85℃	-	-	-40.0	mA
			4.0V≤V_{DD}≤5.5V 85~105℃	-	-	-20.0	
			2.4V≤V_{DD}＜4.0V	-	-	-8.0	mA
			1.8V≤V_{DD}＜2.4V	-	-	-4.0	mA
		Total of P00~P07, P50~P57 (When duty≤70% Note 3)	4.0V≤V_{DD}≤5.5V -40~85℃	-	-	-60.0	mA
			4.0V≤V_{DD}≤5.5V 85~105℃	-	-	-25.0	
			2.4V≤V_{DD}＜4.0V	-	-	-10.0	mA
			1.8V≤V_{DD}＜2.4V	-	-	-5.0	mA
		Total of all pins (When duty≤70% Note 3)	1.8V≤V_{DD}≤5.5V -40~85℃			-100	mA
			1.8V≤V_{DD}≤5.5V 85~105℃	-	-	-45.0	

Note 1: This is the current value that guarantees device operation even if current flows from the V_{DD} pin to the output pin(s).

Note 2: The total current value cannot be exceeded.

Note 3: This is the output current value for the condition “duty cycle≤70%”. The output current value for a duty cycle > 70% can be calculated using the following equation (in the case of changing the duty cycle to n%).

Total output current of pins=(I_{OH}×0.7)/(n×0.01)

<Example>I_{OH}= -10.0mA, n=80%

Total output current of pins= (-10.0×0.7)/(80×0.01) ≈ -8.7mA

The current at each pin does not vary by duty cycle and does not flow above the absolute maximum rating.

Remarks:

1. Unless otherwise specified, the characteristics of multiplexed pins are the same as those of port pins.
2. Low-temperature specification values are guaranteed by the design, and are not tested in mass production.

(T_A= -40~105℃, 1.8V≤V_{DD}≤5.5V, V_{SS}=0V)

Item	Symbol	Condition		Min.	Typ.	Max.	Unit
Output current, low[Note 1]	I_{OL}	Per pin for P00~P07, P10~P17, P20~P25, P30~P37, P40~P47, P50~P57	1.8V≤V_{DD}≤5.5V -40~105℃	-	-	18[Note 2]	mA
		Total of P10~P17, P20~P25, P30~P37, P40~P47 (When duty≤70% [Note 3])	4.0V≤V_{DD}≤5.5V -40~85℃	-	-	50	mA
			4.0V≤V_{DD}≤5.5V 85~105℃	-	-	35	
			2.4V≤V_{DD}＜4.0V	-	-	15	mA
			1.8V≤V_{DD}＜2.4V	-	-	8	mA
		Total of P00~P07, P50~P57 (When duty≤70% [Note 3])	4.0V≤V_{DD}≤5.5V -40~85℃	-	-	60	mA
			4.0V≤V_{DD}≤5.5V 85~105℃	-	-	40	
			2.4V≤V_{DD}＜4.0V	-	-	20	mA
			1.8V≤V_{DD}＜2.4V	-	-	10	mA
		Total of all pins (When duty≤70% [Note 3])	1.8V≤V_{DD}≤5.5V -40~85℃	-	-	80	mA
			1.8V≤V_{DD}≤5.5V 85~105℃	-	-	50	

Note 1: This is the current value guarantees device operation if current flows from the output pin(s) to the V_{SS} pin.

Note 2: The total current value cannot be exceeded.

Note 3: This is the output current value for the condition “duty cycle≤70%”. The output current value for a duty cycle > 70% can be calculated using the following equation (in the case of changing the duty cycle to n%).

Total output current of pins =(I_{OL}×0.7)/(n×0.01)

<Example>I_{OL}=10.0mA, n=80%

Total output current of pins =(10.0×0.7)/(80×0.01) ≈ 8.7mA

The current at each pin does not vary by duty cycle and does not flow above the absolute maximum rating.

Remarks:

1. Unless otherwise specified, the characteristics of multiplexed pins are the same as those of port pins.
2. Low-temperature specification values are guaranteed by the design, and are not tested in mass production.

(T_A= -40~105℃, 1.8V≤V_{DD}≤5.5V, V_{SS}=0V)

Item	Symbol	Condition		Min.	Typ.	Max.	Unit
Input voltage, high	V_{IH}	P00~P07, P10~P17, P20~P25, P30~P37, P40~P47, P50~P57	Schmitt input	0.7V_{DD}	-	V_{DD}	V
Input voltage, low	V_{IL}	P00~P07, P10~P17, P20~P25, P30~P37, P40~P47, P50~P57	Schmitt input	0	-	0.3V_{DD}	V

Item	Symbol	Condition			Min.	Typ.	Max.	Unit
Input voltage, high Input voltage, high	V_{IH}	P00~P07	TTL input	4.0V<V_{DD}<5.5V	2.2	-	V_{DD}	V
				3.3V<V_{DD}<4.0V	2.0	-	V_{DD}	V
				2.5V<V_{DD}<3.3V	1.5	-	V_{DD}	V
Input voltage, low	V_{IL}	P00~P07	TTL input	4.0V<V_{DD}<5.5V	0	-	0.8	V
				3.3V<V_{DD}<4.0V	0	-	0.5	V
				2.5V<V_{DD}<3.3V	0	-	0.32	V

Remarks:

1. Unless otherwise specified, the characteristics of multiplexed pins are the same as those of port pins.
2. Low-temperature specification values are guaranteed by the design, and are not tested in mass production.

(T_A= -40~105℃, 1.8V≤V_{DD}≤5.5V, V_{SS}=0V)

Item	Symbol	Condition		Min.	Typ.	Max.	Unit
Out voltage, high	V_{OH}	P00~P07, P10~P17, P20~P25, P30~P37, P40~P47, P50~P57	4.0V≤V_{DD}≤5.5V, I_{OH1}= -8.0mA	V_{DD}-1.5	-	-	V
			4.0V≤V_{DD}≤5.5V, I_{OH1}= -4.0mA	V_{DD}-0.7	-	-	V
			2.4V≤V_{DD}≤5.5V, I_{OH1}= -2.0mA	V_{DD}-0.6	-	-	V
			1.8V≤V_{DD}≤5.5V, I_{OH1}= -1mA	V_{DD}-0.5	-	-	V
Out voltage, low	V_{OL}	P00~P07, P10~P17, P20~P25, P30~P37, P40~P47, P50~P57	4.0V≤V_{DD}≤5.5V I_{OL1}=18.0mA	-	-	1.2	V
			4.0V≤V_{DD}≤5.5V I_{OL1}=9.0mA	-	-	0.7	V
			2.4V≤V_{DD}≤5.5V I_{OL1}=5.0mA	-	-	0.4	V
			1.8V≤V_{DD}≤5.5V I_{OL1}=2.0mA	-	-	0.4	V

Remarks:

1. Unless otherwise specified, the characteristics of multiplexed pins are the same as those of port pins.
2. Low-temperature specification values are guaranteed by the design, and are not tested in mass production.

(T_A= -40~105℃, 1.8V≤V_{DD}≤5.5V, V_{SS}=0V)

Item	Symbol	Condition		Min.	Typ.	Max.	Unit
Input leakage current, high	I_{LIH}	P00~P07, P10~P17, P20~P25, P30~P37, P40~P47, P50~P57	V_I=V_{DD}	-	-	1	uA
Input leakage current, low	I_{LIL}	P00~P07, P10~P17, P20~P25, P30~P37, P40~P47, P50~P57	V_I=V_{SS}	-	-	-1	uA
On-chip pull-up resistance	R_U	P00~P07, P10~P17, P20~P25, P30~P37, P40~P47, P50~P57	V_I=V_{SS}, in input port	10	30	50	KΩ
On-chip pull-down resistance	R_D	P00~P07, P10~P17, P20~P25, P30~P37, P40~P47, P50~P57	V_I=V_{DD}, in input port	10	30	50	KΩ

Remarks:

1. Unless otherwise specified, the characteristics of multiplexed pins are the same as those of port pins.
2. Low-temperature specification values are guaranteed by the design, and are not tested in mass production.

6.5.2 Supply Current Characteristics

(T_A= -40~105℃, 1.8V≤V_{DD}≤5.5V, V_{SS}=0V)

Item	Symbol	Condition			Min.	Typ.	Max.	Unit
Supply current Note 1	I_{DD1}	Operating mode	High-speed on-chip oscillator	F_{HOCO}=72MHz, F_{IH}=72MHz	-	3.9	4.7	mA
				F_{HOCO}=64MHz, F_{IH}=32MHz	-	3.2	3.7	
			Low-speed on-chip oscillator	F_{IL}=15KHz Note2	-	195	700	uA
	I_{DD2}	Sleep mode	High-speed on-chip oscillator	F_{HOCO}=64MHz, F_{IH}=64MHz	-	1.8	2.2	mA
				F_{HOCO}=32MHz, F_{IH}=32MHz	-	1.2	1.6	
			Low-speed on-chip oscillator	F_{IL}=15KHz Note2	-	60	600	uA
	I_{DD3}Note 3	Deep sleep mode	T_A= -40℃~105℃ V_{DD}=3.0V		-	50	600	uA
		Partial power-down deep sleep mode	T_A = -40℃~25℃ V_{DD}=3.0V		-	30	50	uA
			T_A = -40℃~85℃ V_{DD}=3.0V		-	30	400	
			T_A = -40℃~105℃ V_{DD}=3.0V		-	30	500	

Note 1: This is the current flowing through V_{DD} and includes the input leakage current with the input pin fixed to V_{DD} or V_{SS} state.

Typical value: CPU is in multiplication instruction execution (I_{DD1}), and does not include peripheral operating current.

Maximum value: CPU in multiplication instruction execution (I_{DD1}) and includes peripheral operating current, but does not include the current flowing to the A/D converter, LVD circuit, I/O ports, internal pull-up or pull-down resistors, or the current when rewriting the data flash.

Note 2: This is the case when the high-speed on-chip oscillator stops oscillating.

Note 3: The current flow to 12-bit interval timer and watchdog timer is not included.

Remarks:

1. F_{HOCO}: High-speed on-chip oscillator clock frequency.
2. F_{IH}: High-speed on-chip oscillator system clock frequency.
3. F_{IL}: Low-speed on-chip oscillator clock frequency.
4. Typical ambient temperature: T_A=25℃.
5. Low-temperature specification values are guaranteed by the design, and are not tested in mass production.

(T_A= -40~105℃, 1.8V≤V_{DD}≤5.5V, V_{SS}=0V)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Low-speed on-chip oscillator operating current	I_{FIL} Note 1	-	-	0.2	-	uA
12-bit interval timer operating current	I_{IT} Note 1,2,3	-	-	0.02	-	uA
Watchdog timer operating current	I_{WDT} Note 1,2,4	F_{IL}=15KHz	-	0.22	-	uA
A/D converter operating current	I_{ADC} Note 1,5	ADC @8MHz	-	2.0	-	mA
LVD operating current	I_{LVD} Note 1,6	-	-	0.08	-	uA

Note 1: This is the current flowing through V_{DD}.

Note 2: This is the case when the high-speed on-chip oscillator stops oscillating.

Note 3: This is the current flowing only to the 12-bit interval timer (excluding the current consumption of the low-speed on-chip oscillator). When the 12-bit interval timer is running in normal or sleep mode, the microcontroller's current consumption is the sum of I_{DD1} or I_{DD2} and I_{IT}. Additionally, when the low-speed on-chip oscillator is selected, I_{FIL} must also be added.

Note 4: This is the current flowing to the watchdog timer (including the current consumption of the low-speed on-chip oscillator). When the watchdog timer is running, the microcontroller's current consumption is the sum of I_{DD1} or I_{DD2} or I_{DD3} and I_{WDT}.

Note 5: This is the current flowing to the A/D converter. When the A/D converter is running in normal or sleep mode, the microcontroller's current consumption is the sum of I_{DD1} or I_{DD2} and I_{ADC}.

Note 6: This is the current flowing to the LVD circuit. When the LVD circuit is running, the microcontroller's current consumption is the sum of I_{DD1} or I_{DD2} or I_{DD3} and I_{LVD}.

Remarks:

1. F_{IL}: Low-speed on-chip oscillator clock frequency.
2. Typical ambient temperature: T_A=25℃.
3. Low-temperature specification values are guaranteed by the design, and are not tested in mass production.

6.6 AC Characteristics

(T_A= -40~105℃, 1.8V≤V_{DD}≤5.5V, V_{SS}=0V)

Item	Symbol	Condition		Min.	Typ.	Max.	Unit
Instruction cycle (minimum instruction execution time)	T_{CY}	Main system clock (F_{MAIN}) operation	1.8V≤V_{DD}≤5.5V	0.015625	-	0.5	us
TI00 ~TI03 TI10 ~TI13 inputs high-level width, low-level width	T_{TIH} T_{TIL}	1.8V≤V_{DD}≤5.5V		1/F_{MCK}+10	-	-	ns
TO00 ~ TO03 TO10 ~ TO13 output frequency	F_{TO}	4.0V≤V_{DD}≤5.5V		-	-	16	MHz
		2.4V≤V_{DD}＜4.0V		-	-	8	MHz
		1.8V≤V_{DD}＜2.4V		-	-	4	MHz
CLKBUZ0 CLKBUZ1 output frequency	F_{PCL}	4.0V≤V_{DD}≤5.5V		-	-	16	MHz
		2.4V≤V_{DD}＜4.0V		-	-	8	MHz
		1.8V≤V_{DD}＜2.4V		-	-	4	MHz
Interrupt input high-level width, low-level width	T_{INTH} T_{INTL}	INTP0 ~ INTP3	1.8V≤V_{DD}≤5.5V	1	-	-	us
Key interrupt input high-level width, low-level width	T_{KR}	KR0 ~ KR7	1.8V≤V_{DD}≤5.5V	250	-	-	ns
RESETB low-level width	T_{RSL}	-		10	-	-	us

Remarks:

1. F_{MCK}: Timer4 operating clock frequency.
2. Low-temperature specification values are guaranteed by the design, and are not tested in mass production.

6.7 Analog Characteristics

6.7.1 A/D Converter Characteristics

Classification of A/D converter characteristics

Input channel \ Reference voltage	Reference voltage (+) = V_{DD} Reference voltage (-) = V_{SS}
AN5~AN22	Refer to the table below
Internal reference voltage Temperature sensor output voltage	

1) When reference voltage(+)=V_{DD}, reference voltage(-)=V_{SS}

(T_A= -40~105℃, 2.5V≤V_{DD}≤5.5V, V_{SS}=0V, reference voltage(+)=V_{DD}, reference voltage(-)=V_{SS})

Item	Symbol	Condition		Min.	Typ.	Max.	Unit
Resolution	RES			-	12	-	bit
Overall error Note 1	AINL	12-bit resolution	2.5V≤V_{DD}≤5.5V	-	6	-	LSB
Conversion time Note3	T_{CONV}	12-bit resolution Target pin: AN5~AN22	2.5V≤V_{DD}≤5.5V	-	52	-	Tmclk
Zero-scale error Note1	E_{ZS}	12-bit resolution	2.5V≤V_{DD}≤5.5V	-	0	-	LSB
Full-scale error Note 1	E_{FS}	12-bit resolution	2.5V≤V_{DD}≤5.5V	-	0	-	LSB
Integral linearity error Note 1	ILE	12-bit resolution	2.5V≤V_{DD}≤5.5V	-	-	±2	LSB
Differential linearity error Note 1	DLE	12-bit resolution	2.5V≤V_{DD}≤5.5V	-	-	±3	LSB
Analog input voltage	V_{AIN}	AN5~AN22		0	-	V_{DD}	V
		Internal reference voltage (2.5V≤V_{DD}≤5.5V)		V_{BGR} Note 2			V
		Temperature sensor output voltage (2.5V≤V_{DD}≤5.5V)		V_{TMPS25} Note 2			V

Note 1: Excludes quantization error (±1/2 LSB).

Note 2: Refer to “6.7.2 Characteristics of temperature sensor/internal reference voltage”.

Note 3: T_{MCLK} is the action clock period of AD, and the maximum action frequency is 8MHz.

Remark: Low-temperature specification values are guaranteed by the design, and are not tested in mass production.

6.7.2 Characteristics of Temperature Sensor/Internal Reference Voltage

(T_A= -40~105℃, 2.5V≤V_{DD}≤5.5V, V_{SS}=0V)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Temperature sensor output voltage	V_{TMPS25}	ADS register =80H, T_A=25℃	-	1.09	-	V
Internal reference voltage	V_{BGR}	ADS register =81H	1.38 Note 1	1.45	1.5 Note 1	V
Internal ADCLDO	$V_{ADCLDO1}$		3.52	3.6	3.68	V
Internal ADCLDO	$V_{ADCLDO2}$		4.11	4.2	4.29	V
Temperature coefficient	F_{VTMPS}	-	-	-3.5	-	mV/℃
Operation stabilization wait time	T_{AMP}	-	5	-	-	us

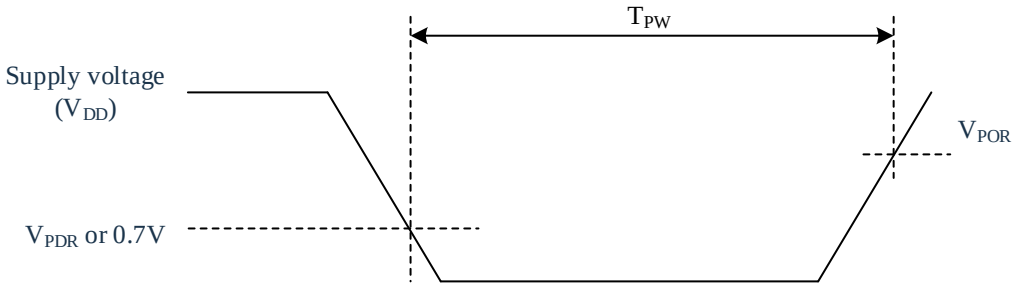
Note 1: Low-temperature specification values are guaranteed by the design, and are not tested in mass production.

6.7.3 POR Circuit Characteristics

(T_A= -40~105℃, V_{SS}=0V)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Detection voltage	V_{POR}	The power supply voltage is rising	-	1.50	1.75	V
	V_{PDR}	The power supply voltage is falling	1.37	1.45	-	V
Minimum pulse width Note 1	T_{PW}	-	300	-	-	us

Note 1: Minimum time required for a POR reset when V_{DD} exceeds below V_{PDR}. This is also the minimum time required for a POR reset from when V_{DD} exceeds below 0.7V to when V_{DD} exceeds V_{POR} while deep sleep mode is entered or the main system (F_{MAIN}) clock is stopped through setting bit0 (HIOSTOP) and bit7 (MSTOP) in the clock status control register (CSC).



Remark: Low-temperature specification values are guaranteed by the design, and are not tested in mass production.

6.7.4 LVD Circuit Characteristics

1. Reset mode, interrupt mode

(T_A= -40~105℃, V_{PDR}≤V_{DD}≤5.5V, V_{SS}=0V)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Detection voltage	V_{LVD0}	The power supply voltage is rising.	-	4.06	4.14	V
		The power supply voltage is falling.	3.90	3.98	-	V
	V_{LVD1}	The power supply voltage is rising.	-	3.75	-	V
		The power supply voltage is falling.	-	3.67	-	V
	V_{LVD2}	The power supply voltage is rising.	-	3.13	-	V
		The power supply voltage is falling.	-	3.06	-	V
	V_{LVD3}	The power supply voltage is rising.	-	3.02	-	V
		The power supply voltage is falling.	-	2.96	-	V
	V_{LVD4}	The power supply voltage is rising.	-	2.92	-	V
		The power supply voltage is falling.	-	2.86	-	V
	V_{LVD5}	The power supply voltage is rising.	-	2.81	-	V
		The power supply voltage is falling.	-	2.75	-	V
	V_{LVD6}	The power supply voltage is rising.	-	2.71	-	V
		The power supply voltage is falling.	-	2.65	-	V
	V_{LVD7}	The power supply voltage is rising.	-	2.61	-	V
		The power supply voltage is falling.	-	2.55	-	V
	V_{LVD8}	The power supply voltage is rising.	-	2.50	-	V
		The power supply voltage is falling.	-	2.45	-	V
	V_{LVD9}	The power supply voltage is rising.	-	2.09	-	V
		The power supply voltage is falling.	-	2.04	-	V
	V_{LVD10}	The power supply voltage is rising.	-	1.98	-	V
		The power supply voltage is falling.	-	1.94	-	V
	V_{LVD11}	The power supply voltage is rising.	-	1.88	1.91	V
		The power supply voltage is falling.	1.80	1.84	-	V
Minimum pulse width	T_{LW}	-	300	-	-	us
Detection delay time	-	-	-	-	300	us

Remark: Low-temperature specification values are guaranteed by the design, and are not tested in mass production.

2. Interrupt & reset mode

(T_A= -40~105℃, V_{PDR}≤V_{DD}≤5.5V, V_{SS}=0V)

Item	Symbol	Condition			Min.	Typ.	Max.	Unit
Interrupt & reset mode	V_{LVDA0}	V_{POC2}=0 V_{POC1}=0 V_{POC0}=0	Falling reset voltage		1.60	1.63	-	V
	V_{LVDA1}		LVIS1=1 LVIS0=0	Rising release reset voltage	-	1.77	1.81	V
				Falling interrupt voltage	1.70	1.73	-	V
	V_{LVDA2}		LVIS1=0 LVIS0=1	Rising release reset voltage	-	1.88	-	V
				Falling interrupt voltage	-	1.84	-	V
	V_{LVDA3}		LVIS1=0 LVIS0=0	Rising release reset voltage	-	2.92	-	V
				Falling interrupt voltage	-	2.86	-	V
	V_{LVDB0}	V_{POC2}=0 V_{POC1}=0 V_{POC0}=1	Falling reset voltage			1.84	-	V
	V_{LVDB1}		LVIS1=1 LVIS0=0	Rising release reset voltage	-	1.98	-	V
				Falling interrupt voltage	-	1.94	-	V
	V_{LVDB2}		LVIS1=0 LVIS0=1	Rising release reset voltage	-	2.09	-	V
				Falling interrupt voltage	-	2.04	-	V
	V_{LVDB3}		LVIS1=0 LVIS0=0	Rising release reset voltage	-	3.13	-	V
				Falling interrupt voltage	-	3.06	-	V
	V_{LVDC0}	V_{POC2}=0 V_{POC1}=1 V_{POC0}=0	Falling reset voltage			2.45	-	V
	V_{LVDC1}		LVIS1=1 LVIS0=0	Rising release reset voltage	-	2.61	-	V
				Falling interrupt voltage	-	2.55	-	V
	V_{LVDC2}		LVIS1=0 LVIS0=1	Rising release reset voltage	-	2.71	-	V
				Falling interrupt voltage	-	2.65	-	V
	V_{LVDC3}		LVIS1=0 LVIS0=0	Rising release reset voltage	-	3.75	-	V
				Falling interrupt voltage	-	3.67	-	V
	V_{LVDD0}	V_{POC2}=0 V_{POC1}=1 V_{POC0}=1	Falling reset voltage		-	2.75	-	V
	V_{LVDD1}		LVIS1=1 LVIS0=0	Rising release reset voltage	-	2.92	-	V
				Falling interrupt voltage	-	2.86	-	V
	V_{LVDD2}		LVIS1=0 LVIS0=1	Rising release reset voltage	-	3.02	-	V
				Falling interrupt voltage	-	2.96	-	V
	V_{LVDD3}		LVIS1=0 LVIS0=0	Rising release reset voltage	-	4.06	4.14	V
				Falling interrupt voltage	3.90	3.98	-	V

Remark: Low-temperature specification values are guaranteed by the design, and are not tested in mass production.

6.7.5 Power Supply Voltage Rising Slope Characteristics

(T_A= -40~105℃, V_{SS}=0V)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Power supply voltage rising slope	S_{VDD}	-	-	-	54	V/ms

Remark: Low-temperature specification values are guaranteed by the design, and are not tested in mass production.

6.7.6 ACMP0/1 Electrical Parameters

T_A=25℃, V_{SENSE}=V_{IN+}-V_{IN-}, V_{DD}=5V, V_{IN+}=1V, unless otherwise specified.

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
V_{DD}	Supply voltage	-	2.1	-	5.5	V
I_Q	Quiescent current	V_{SENSE}=0.1V	-	0.3	0.4	mA
I_{SD}	Shutdown current	V_{SENSE}=0.1V	-	5	-	nA
T_A	Operating temperature	-	-40	25	105	℃
Input characteristics						
V_{OS}	Input offset voltage	-	-10.0	±4.0	10.0	mV
V_{CM}	Common mode input voltage range	-40℃~105℃	-0.1	-	V_{DD}	V
I_B	Input bias current	V_{SENSE}=0mV	-	10	-	pA
I_{OS}	Input offset current	V_{SENSE}=0mV	-	10	-	pA
V_{HYS}	Input hysteresis voltage	V_{DD}=2.1~5.5V, V_{IN+}=0.5V	-	0 ±10 ±20 ±60	-	mV
Output characteristics						
V_{OH}	Maximum output voltage	-40℃~105℃	-	-	V_{DD}	V
V_{OL}	Minimum output voltage	-40℃~105℃	0	-	-	V
Frequency characteristics						
A_{OL}	Open loop gain	-	-	80	-	dB
BW	Bandwidth	-	-	120	-	MHz
PSRR	Power supply rejection ratio	V_{DD}=2.1~5.5V, V_{IN+}=1V, V_{SENSE}=0mV	-	80	-	dB
CMRR	Common mode rejection ratio	V_{DD}=2.1~5.5V, -40℃~105℃	-	90	-	dB
Transient characteristics						
T_{STB}	Stabilization time	-	-	-	2	μs
T_{PGD}	Response delay	V_{COM}=1V, V_{IN+}= V_{IN-} ±0.1V	-	50	100	ns

Remark: This specification is guaranteed by the design, and is not tested in mass production.

6.7.7 PGA0/1/2/3 Electrical Parameters

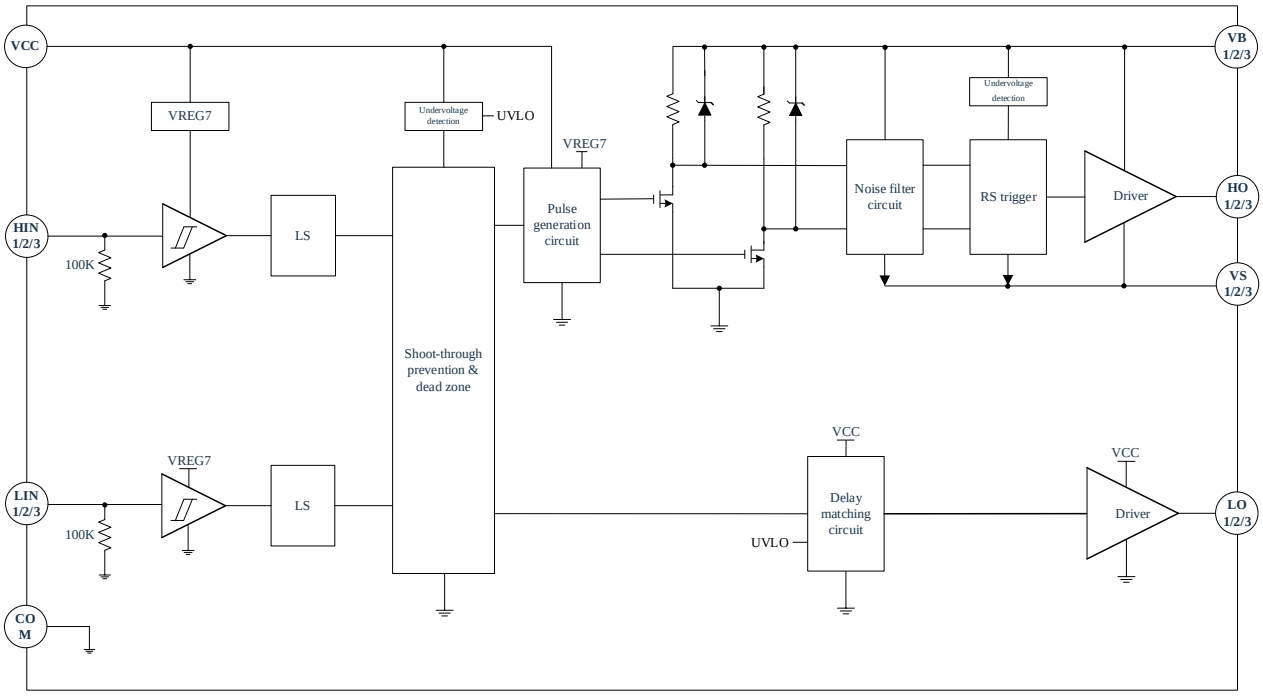
T_A＝25℃, V_{DD}＝5V, V_{IN+}=0.1V, unless otherwise specified (G is the gain multiplier).

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
V_{DD}	Supply voltage	-	2.5	-	5.5	V
I_Q	Quiescent current	V_{OUT}=2V	-	0.9	1.5	mA
I_{SD}	Shutdown current	-	-	10	-	nA
T_A	Operating temperature	-	-40	25	105	℃
Input characteristics						
V_{OS}	Input offset voltage	-	-25	-	25	mV
V_{CM}	Common mode input voltage range	-40℃~105℃, G≥2	0.35 /G	-	(V_{DD}-0.35)/ G	V
I_B	Input bias current	-	-	10	-	pA
I_{OS}	Input offset current	-	-	10	-	pA
Output characteristics						
EG	Error gain		-3	-	3	%
C_{LOAD}	Capacitive load	G=1, 2.5, 5, 7, 7.5, 10, 15	-	10	-	pF
V_{OH}	Maximum output voltage	-40℃~105℃	-	V_{DD}-0.35	-	V
V_{OL}	Minimum output voltage	-40℃~105℃	-	0.35	-	V
V_{A0O} V_{A1O} V_{A2O}	Test output port of PGA0/1/2 (A0O, A1O, A2O)	-40℃~105℃ Output port unloaded	-	-	V_{DD}-0.35	V
Frequency characteristics						
BW	Bandwidth	R_{LOAD}=2KΩ, C_{LOAD}=100pF G=1	-	10	-	MHz
PSRR	Power supply rejection ratio	V_{DD}=2.5~5.5V	-	60	-	dB
CMRR	Common mode rejection ratio	-40℃~105℃	-	80	-	dB
Transient characteristics						
SR	Slew rate	R_{LOAD}=2KΩ, C_{LOAD}=100pF G=1	-	15	-	V/μs
T_{STB}	Stabilization time	-	-	-	2	μs

Remark: This specification is guaranteed by the design, and is not tested in mass production.

6.8 Gate Driver (6N) Electrical Characteristics (CMS32M6736EGH48NB/ CMS32M6736EGH48FA/CMS32M6734EGH48FA)

6.8.1 Internal Logic Block Diagram



6N pre-drive internal logic block diagram

6.8.2 Absolute Maximum Ratings

(T_A=25℃, all pins are referenced to GND unless otherwise specified).

Parameter		Symbol	Min.	Max.	Unit
High-side floating offset absolute voltage		$VB_{1,2,3}$	-0.3	225	V
High-side floating offset relative voltage		$VS_{1,2,3}$	$VB_{1,2,3}$-25	$VB_{1,2,3}$+0.3	V
High-side output voltage		$VHO_{1,2,3}$	VS1,2,3-0.3	$VB_{1,2,3}$+0.3	V
Max power supply voltage		VCC	-0.3	25	V
Low-side output voltage		$V_{LO1,2,3}$	-0.3	VCC+0.3	V
Maximum input voltage (HIN1,2,3/LIN1,2,3)		V_{IN}	-0.3	15	V
Maximum offset voltage slew rate		dVS/dt	-	50	V/ns
Junction-to-ambient thermal resistance (Note 1)	QFN48	θ_{JA}	-	100	℃/W
	LQFP48		-	52	
Junction temperature		T_J	-	150	℃
Storage temperature		T_s	-55	150	℃
Pin soldering temperature (Duration: 10s)		T_L	-	260	℃
ESD_HBM (Note 2)		V_{ESD1}	-	2000	V
ESD_CDM		V_{ESD2}	-	750	V

Note 1: T_A is the operating temperature of the circuit, θ_{JA} is the package thermal resistance, 150℃ is the maximum operating junction temperature of the circuit.

Note 2: Human body model, 100pF capacitance discharged through a 1.5kΩ resistor.

Remark: Exceeding the absolute maximum ratings may cause permanent damage to the chip.

6.8.3 Recommended Operating Conditions

(T_A=25℃, all pins are referenced to GND unless otherwise specified).

Parameter	Symbol	Min.	Typ.	Max.	Unit
High-side floating offset absolute voltage	$VB_{1,2,3}$	$VS_{1,2,3}$+5	$VS_{1,2,3}$+15	$VS_{1,2,3}$+20	V
High-side floating offset relative voltage	$VS_{1,2,3}$	GND-5	-	200	V
High-side output voltage	$V_{HO1,2,3}$	$VS_{1,2,3}$	$VS_{1,2,3}$+15	$VB_{1,2,3}$	V
Supply voltage	VCC	5	15	20	V
Low-side output voltage	$V_{LO1,2,3}$	0	15	VCC	V
Input voltage (HIN1,2,3/LIN1,2,3)	V_{IN}	0	-	5	V

Remark: T_A represents the operating temperature of the circuit.

6.8.4 Table of Electrical Characteristics

(T_A=25℃, VCC=$VBS_{1,2,3}$=15V, $VS_{1,2,3}$=GND, all pins are referenced to GND unless otherwise specified).

Parameter	Symbol	Test condition	Min.	Typ.	Max.	Unit
Power supply current parameters						
VCC quiescent current	I_{CCQ}	V_{IN}=0V	72	81	89	uA
VBS quiescent current	I_{BSQ}	V_{HIN}=0V	27	30	33	uA
VCC dynamic current	I_{CCD}	$f_{LIN1,2,3}$=20kHz	300	319	360	uA
VBS dynamic current	I_{BSD}	$f_{HIN1,2,3}$=20kHz	113	125	132	uA
VB shift current	$I_{VB\_shift\_tr}$	-	5.6	6.0	15.0	mA
VB floating supply leakage current	I_{LK}	VB=VS=200V	-	-	1	uA
Power supply voltage parameters						
VCC undervoltage high level potential	VCC_{HY+}		-	4.2	4.8	V
VCC undervoltage low level potential	VCC_{HY-}		3.4	3.8	-	V
VCC undervoltage hysteresis level	VCC_{HY}		-	0.4	-	V
VBS undervoltage high level potential	VBS_{HY+}		-	3.8	4.3	V
VBS undervoltage low level potential	VBS_{HY-}		3.0	3.5	-	V
VBS undervoltage hysteresis level	VBS_{HY}		-	0.3	-	V
VS quiescent negative voltage	VS_{QN}	VBS=15V	-	-5.0	-	V
Input parameters						
Input high level current	I_{IN+}	V_{IN}=5V	47	50	53	uA
Input low level current	I_{IN-}	V_{IN}=0V	-	0	-	uA
Input high level potential	V_{IN+}		2.6	-	-	V
Input low level potential	V_{IN-}		-	-	1.1	V
Input hysteresis level	V_{INHY}		-	1.0	-	V
Output parameters						
High-level short-circuit pulse current	I_{OUT+}	V_{IN}=5V, V_O=0V, PWD≤10us	-	1.2	-	A
Low-level short-circuit pulse current	I_{OUT-}	V_{IN}=0V, V_O=15V, PWD≤10us	-	1.2	-	A
High-level output voltage	V_{OUT+}	I_{OUT}=100mA	-	0.8	-	V
Low-level output	V_{OUT-}	I_{OUT}=100mA	-	0.3	-	V

voltage						
Time parameters						
Output rise edge transfer time	t_{ON}	No Load	130	140	160	ns
Output fall edge transfer time	t_{OFF}	No Load	130	140	160	ns
Output rise time	t_r	C_L=3.3nF	47	60	73	ns
Output fall time	t_f	C_L=3.3nF	36	45	56	ns
Dead time	DT	No Load	328	350	378	ns
High-side/low-side matching time	MT		-	-	50	ns
VB shift current pulse time	t_{r_width}	-	240	300	500	ns
BRK input filter time	t_{FLT}	V_{BRK}=0/5V	45	60	75	ns
BRK turn-on time	T_{on_BRK}	V_{BRK}=5V	120	130	160	ns
BRK turn-off time	T_{off_BRK}	V_{BRK}=0V	120	130	160	ns

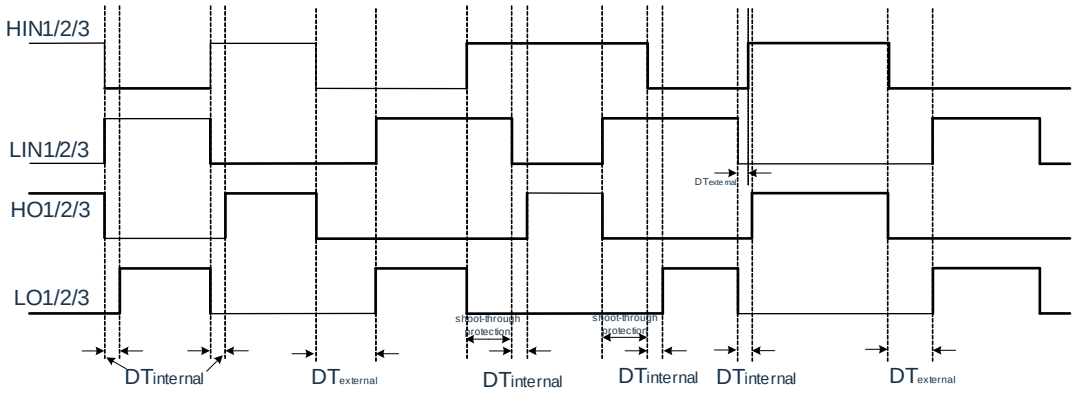
6.8.5 Logic Timing Diagram

The chip has a built-in fixed dead-time protection circuit. During the dead-time, both the high-side and low-side outputs are set to a low level. The set dead-time must ensure that one power transistor is fully turned off before the other is turned on, preventing a shoot-through phenomenon between the transistors.

If the external dead-time $DT_{external}$ is less than the internal minimum dead-time $DT_{internal}$, then $DT_{internal}$ will be the dead-time for the driver output.

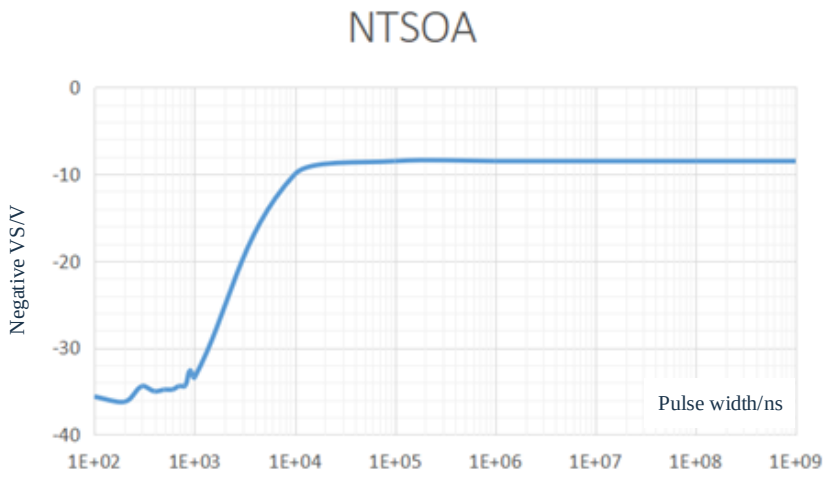
If the external dead-time $DT_{external}$ is greater than the internal minimum dead-time $DT_{internal}$, then $DT_{external}$ will be the dead-time for the driver output.

The chip also includes a protection circuit specifically designed to prevent shoot-through of power transistors. It can effectively prevent damage caused by shoot-through when the high-side and low-side input signals are interfered with. The following diagram illustrates the timing relationship between the dead-time, input signals, driver output signals, and shoot-through protection circuit.



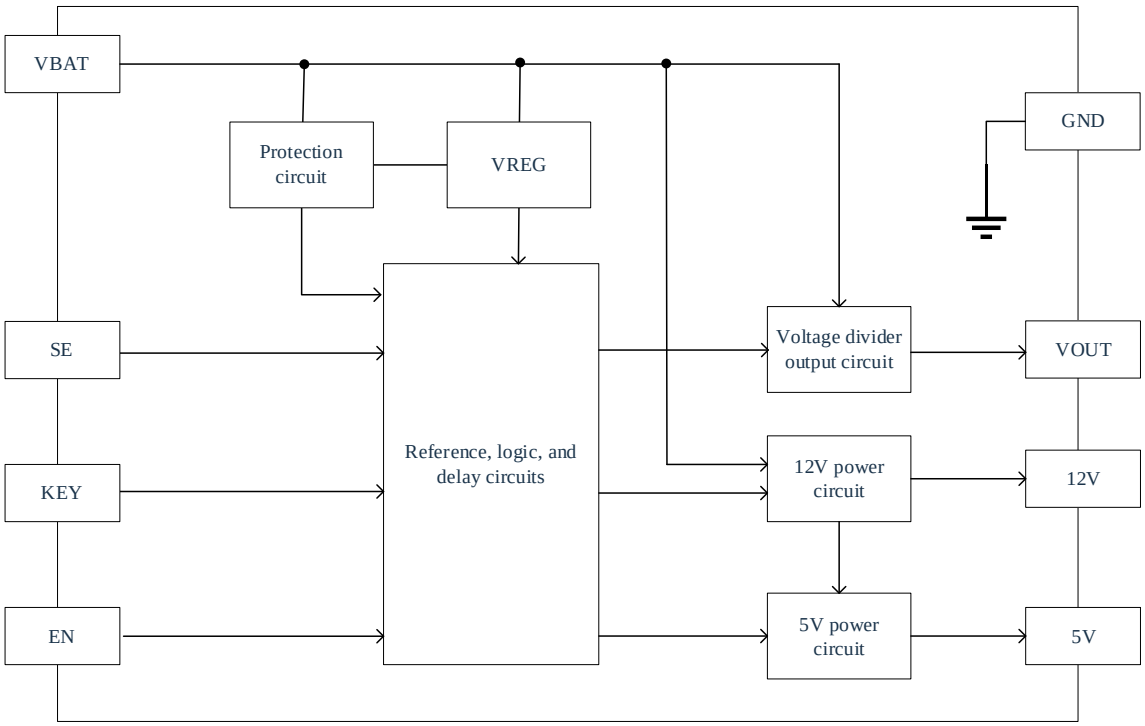
6.8.6 Negative Transient Safe Operating Area (NTSOA)

The Negative Transient Safe Operating Area (NTSOA) characterizes the gate driver's ability to handle transient negative voltages. Negative pulses with amplitude and pulse width above the blue line shown in the diagram below allow the gate driver to operate normally. Pulses with excessively large amplitudes (located below the blue line) may cause the gate driver to malfunction or even result in permanent damage.

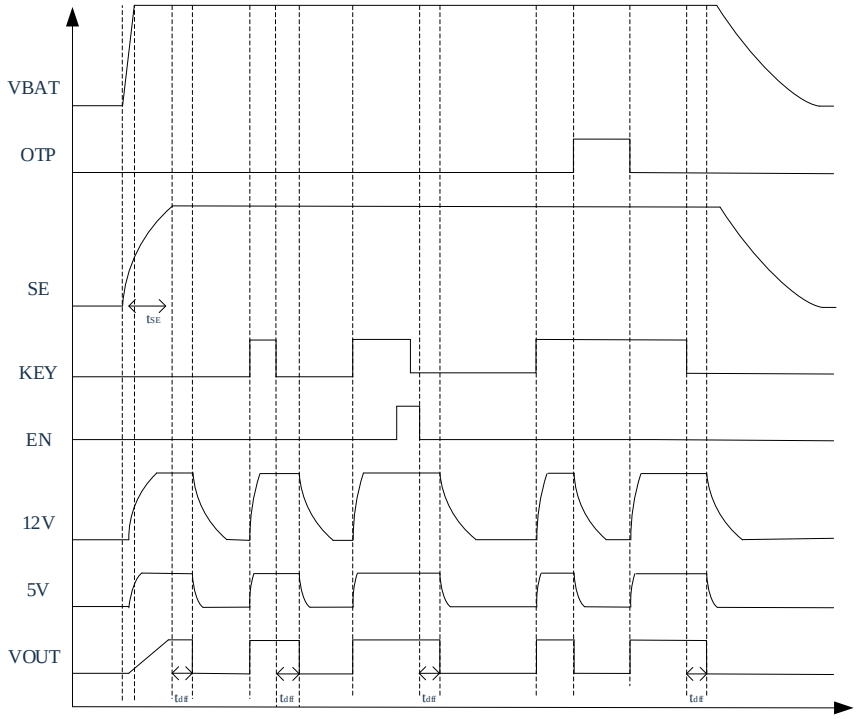


6.9 LDO Electrical Characteristics (CMS32M6734EGH48FA)

6.9.1 Internal Block Diagram



LDO internal block diagram



Logic timing diagram

6.9.2 Absolute Maximum Ratings

(T_A=25℃, all pins are referenced to GND unless otherwise specified).

Parameter	Symbol	Min.	Max.	Unit
Maximum supply voltage	VBAT	-0.3	40	V
SE maximum voltage	VSE	-0.3	V_{BAT}+0.3	V
KEY maximum voltage	VKEY	-0.3	V_{BAT}+0.3	V
EN maximum voltage	V_{EN}	-0.3	6	V
12V max. continuous output current	I_{12V}	0	100	mA
5V max. continuous output current	I_{5V}	0	60	mA

Note 1: T_A indicates the circuit operating temperature.

6.9.3 Recommended Operating Conditions

(T_A=25℃, V_{BAT}=21V, all pins are referenced to GND unless otherwise specified).

Parameter	Symbol	Condition	Min.	Max.	Unit
Input voltage	VBAT		6	36	V
SE input voltage	V_{SE}		0	VBAT	V
KEY input voltage	VKEY		0	VBAT	V
EN input voltage	V_{EN}		0	5	V
12V continuous output current	I_{12V}	SE=0V/KEY=VBAT	0	60	mA
5V continuous output current	I_{5V}	SE=0V/KEY=VBAT	0	30	mA

Note 1: T_A indicates the circuit operating temperature.

6.9.4 Table of Electrical Characteristics

(T_A=25℃, V_{BAT}=21V, all pins are referenced to GND unless otherwise specified).

Parameter	Symbol	Test condition	Min.	Typ.	Max.	Unit
Power supply parameters						
Power supply undervoltage positive threshold	$VBAT_{\_UVLO+}$	SE=0V/KEY=VBAT	-	5.3	-	V
Power supply undervoltage negative threshold	$VBAT_{\_UVLO-}$	SE=0V/KEY=VBAT	-	4.6	-	V
Operating current	I_{VCC}	SE=0V/KEY=VBAT/EN=5V	0.92	1.2	1.73	mA
Standby current	I_Q	SE=VBAT/KEY=0V/EN=0V	-	-	1	uA
Input parameters						
KEY high-level input current	I_{KEY}	VKEY=5V	20	45	60	uA
KEY undervoltage threshold positive voltage	$VKEY_{\_UV+}$	VKEY=VBAT	-	2.5	-	V
EN high level input current	I_{EN}	V_{EN}=5V	-	35	-	uA
EN high level	V_{EN_H}		2.5	-		V
EN low level	V_{EN_L}		-	-	0.8	V
SE voltage	V_{SE}	SE floating voltage	-		VBAT	V
SE charge time	t_{SE}	SE external capacitor 1nF	-	400	-	us
12V power supply parameters						
Output voltage	V_{12V}	SE=0V/KEY=VBAT/EN=5V	11.8	12.0	12.2	V
Rated load current	I_{load12}	SE=0V/KEY=VBAT/EN=5V	-	-	60	mA
Line regulation	ΔV_line12	SE=0V/KEY=VBAT/EN=5V VBAT=13~30V, I_{load12}=60mA	-	-	10	mV
Load regulation	ΔV_load12	SE=0V/KEY=VBAT/EN=5V I_{load12}=0~60mA	-	33	60	mV
Power supply rejection ratio	PSRR_12V	SE=0V/KEY=VBAT/EN=5V ΔVBAT=5V, f=1kHz	40	-	-	dB
Temperature drift	ΔV_temp12	SE=0V/KEY=VBAT/EN=5V T_A=-20℃~85℃, I_{load12}=10mA	-	-	100	mV
Minimum dropout voltage	V_{DO_12V}	SE=0V/KEY=VBAT/EN=5V I_{load12}=100mA, 12V output drops by 3%.	150	250	450	mV
Current limit point	I_limit12		-	230	-	mA

Parameter	Symbol	Test condition	Min.	Typ.	Max.	Unit
5V power supply parameters						
Output voltage	V_{5V}	SE=0V/KEY=VBAT/EN=5V	4.95	5.00	5.05	V
Rated load current	I_{load5}	SE=0V/KEY=VBAT/EN=5V	-	-	30	mA
Line regulation	ΔV_line5	SE=0V/KEY=VBAT/EN=5V, VBAT=13~25V, I_{load5}=30mA	-	-	10	mV
Load regulation	ΔV_load5	SE=0V/KEY=VBAT/EN=5V, I_{load5}=0~60mA	-	38	65	mV
Power supply rejection ratio	PSRR_5V	SE=0V/KEY=VBAT/EN=5V, ΔVBAT=5V, f=1kHz	40	-	-	dB
Temperature drift	ΔV_temp5	SE=0V/KEY=VBAT/EN=5V, TA=-20℃~85℃, I_{load5}=10mA	20	35	50	mV
Minimum voltage drop	V_{DO_5V}	SE=0V/KEY=VBAT/EN=5V, I_{load5}=30mA, 12V output drops by 3%	200	330	550	mV
Current limit point	I_limit5		-	122	-	mA
Voltage divider output parameters						
Voltage divider output	V_{OUT}	SE=0V/KEY=VBAT/EN=5V	-	1.91	-	V
Voltage divider output ratio	R_{OUT}	V_{OUT}/VBAT	-	1/11	-	
Protection functions						
Over-temperature protection positive threshold	T_{OTP+}	SE=0V/KEY=VBAT/EN=5V	-	160	-	℃
Over-temperature protection negative threshold	T_{OTP-}	SE=0V/KEY=VBAT/EN=5V	-	140	-	℃
Output delay shutdown	t_{dff}	SE=VBAT/KEY=0V/EN=0V	11	16	21	ms

6.10Memory Characteristics

6.10.1 Flash Memory

(T_A= -40~105℃, 1.8V≤V_{DD}≤5.5V, V_{SS}=0V)

Symbol	Parameter	Test condition	Min.	Max.	Unit
T_{PROG}	Word write time (32bit)	T_A= -40~105℃	-	120	us
T_{ERASE}	Sector erase time (512B)	T_A= -40~105℃	2	3	ms
	Chip erase time	T_A= -40~105℃	30	40	ms
N_{END}	Number of rewritable times	T_A= -40~105℃	100	-	Kcycles
T_{RET}	Data retention period	100 kcycles Note 1 at T_A =125℃	20	-	Years

Note 1: Cycling tests are performed within the temperature range.

Remark: Low-temperature specification values are guaranteed by the design, and are not tested in mass production.

6.10.2 RAM Memory

(T_A= -40~105℃, 1.8V≤V_{DD}≤5.5V, V_{SS}=0V)

Symbol	Parameter	Test condition	Min.	Max.	Unit
$V_{RAMHOLD}$	RAM hold voltage	T_A= -40~105℃	0.8	-	V

Remark: Low-temperature specification values are guaranteed by the design, and are not tested in mass production.

6.11EMS Characteristics

6.11.1 ESD Electrical Characteristics

Symbol	Parameter	Test condition	Grade
$V_{ESD(HBM)}$	Electrostatic discharge (Human-Body Model HBM)	T_A = 25℃, ANSI/ESDA/JEDEC JS-001-2017	3B
	Electrostatic discharge (Charged-Device Model CDM)	T_A = 25℃, ANSI/ESDA/JEDEC JS-002-2022	C3

Remark: This specification is guaranteed by the design, and is not tested in mass production.

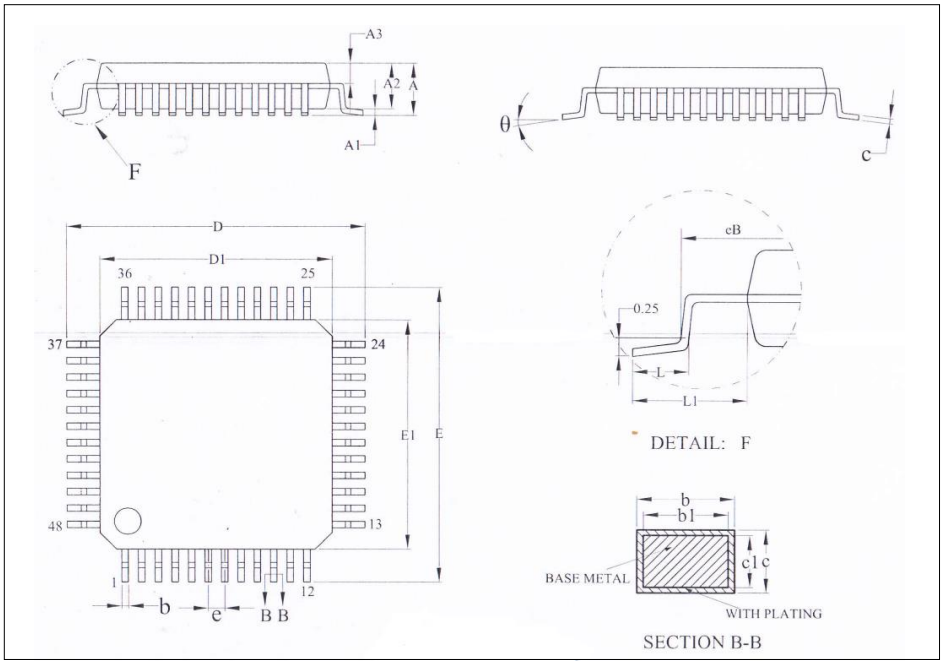
6.11.2 Latch-Up Electrical Characteristics

Symbol	Parameter	Test condition	Level
LU	Static latch-up class	JESD78F	Class I A (T_A = +25℃)

Remark: This specification is guaranteed by the design, and is not tested in mass production.

7. Package Dimensions

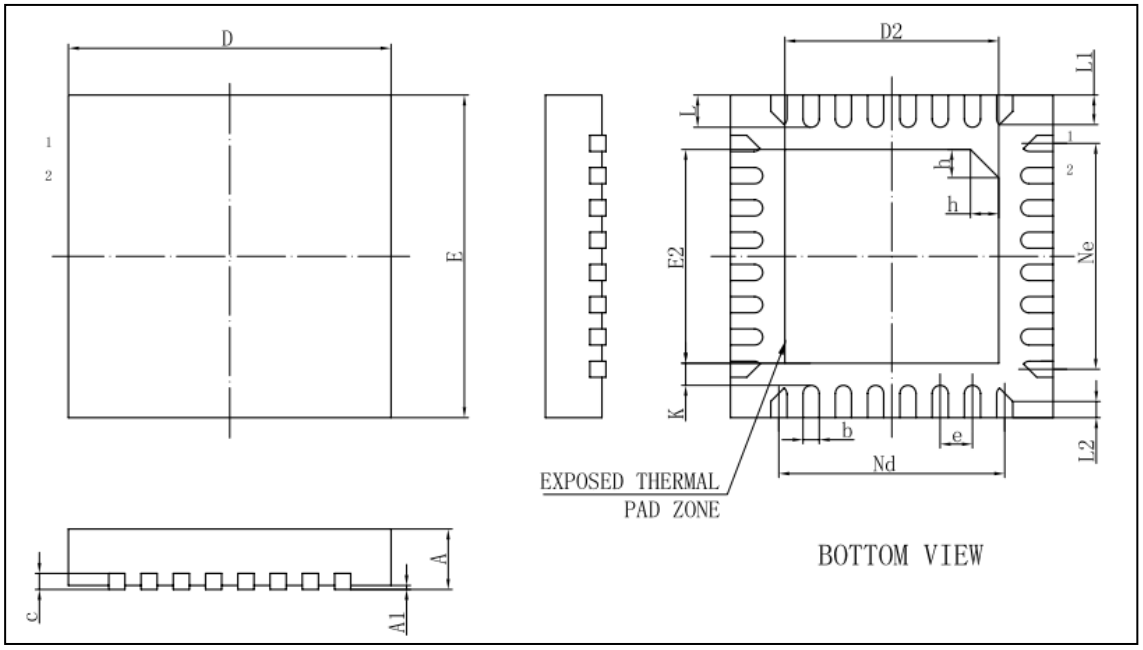
7.1 LQFP48L (7.0x7.0mm, 0.5mm)



Symbol	Millimeter		
	Min	Nom	Max
A	-	-	1.60
A1	0.05	-	0.15
A2	1.30	1.40	1.50
A3	0.59	0.64	0.69
b	0.18	-	0.26
b1	0.17	0.20	0.23
c	0.13	-	0.18
c1	0.12	0.13	0.14
D	8.80	9.00	9.20
D1	6.90	7.00	7.10
E	8.80	9.00	9.20
E1	6.90	7.00	7.10
eB	8.10	-	8.25
e	0.50BSC		
L	0.43	-	0.75
L1	1.00REF		
θ	0	-	8°

Caution: Package dimensions do not include mold flash or gate burrs.

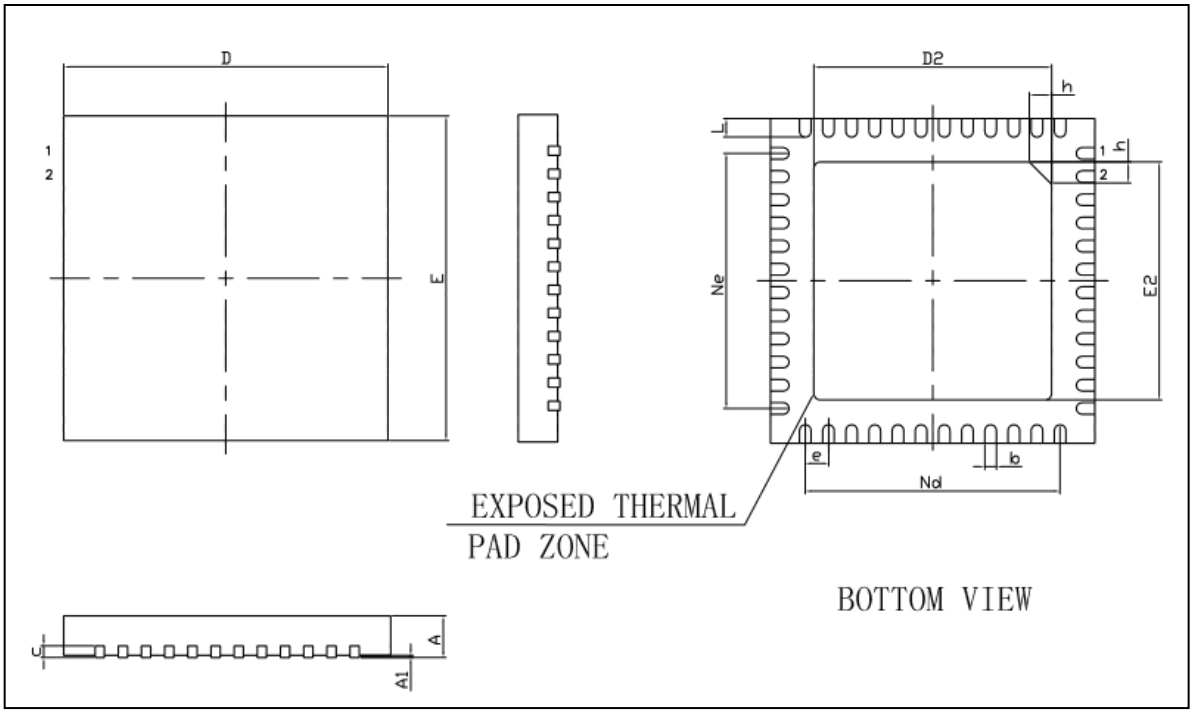
7.2 QFN32 (4.0x4.0mm, 0.4mm)



Symbol	Millimeter		
	Min	Nom	Max
A	0.70	0.75	0.80
A1	0	0.02	0.05
b	0.15	0.20	0.25
c	0.18	0.20	0.25
D	3.90	4.00	4.10
D2	2.60	2.65	2.70
e	0.40BSC		
Ne	2.80BSC		
Nd	2.80BSC		
E	3.90	4.00	4.10
E2	2.60	2.65	2.70
L	0.35	0.40	0.45
L1	0.30	0.35	0.40
L2	0.15	0.20	0.25
h	0.30	0.35	0.40

Caution: Package dimensions do not include mold flash or gate burrs.

7.3 QFN48 (6.0x6.0mm, 0.4mm)



Symbol	Millimeter		
	Min	Nom	Max
A	0.70	0.75	0.80
A1	-	0.02	0.05
b	0.15	0.20	0.25
c	0.18	0.20	0.23
D	5.90	6.00	6.10
D2	4.10	4.20	4.30
e	0.40BSC		
Ne	4.40BSC		
Nd	4.40BSC		
E	5.90	6.00	6.10
E2	4.10	4.20	4.30
L	0.35	0.40	0.45
h	0.30	0.35	0.40

Caution: Package dimensions do not include mold flash or gate burrs.

8. Ordering Information

Product model	Core	Clock frequency (MHZ)	Program FLASH(KB)	Data FLASH (KB)	SRAM(KB)	Internal driver	WDT	Timer	Universal timer	GPIO	12-Bit ADC	DAC	Intemal PGA	Intemal CMP	EPWM	CCP	UART	I2C	SPI	Temnperature sensor	CRC	DIVSQRT	DIV	EDMA	HALL signal processing	Drive power/V	Gate float voltage withstand /V	LDO/V	PACKAGE
CMS32M6710GH32NB	M0+	72	128	1	12	-	1	2	4	30	21	1	4	2	6	2	2	1	1	1	1	1	1	1	1	-	-	-	QFN32
CMS32M6710GH48FA	M0+	72	128	1	12	-	1	2	4	46	27	1	4	2	8	2	2	1	1	1	1	1	1	1	1	-	-	-	LQFP48
CMS32M6736EGH48NB	M0+	72	128	1	12	6N	1	2	4	32	25	1	4	2	6	2	2	1	1	1	1	1	1	1	1	5-20	200	-	QFN48
CMS32M6736EGH48FA	M0+	72	128	1	12	6N	1	2	4	32	25	1	4	2	6	2	2	1	1	1	1	1	1	1	1	5-20	200	-	LQFP48
CMS32M6734EGH48FA	M0+	72	128	1	12	6N	1	2	4	26	22	1	3	2	6	2	2	1	1	1	1	1	1	1	1	5-20	200	5+12	LQFP48

9. Revision History

Version #	Date	Description of changes
V1.0.0	Aug. 2023	Formal version 1) Removed the CMS32M6734GH48FA model and related information. 2) Added the CMS32M6734EGH48FA model and related information. 3) Updated section 1.3. 4) Updated the parameters in sections 6.8.2, 6.8.3, 6.8.4, 6.9.2, 6.9.3, 6.9.4, and 6.11. 5) Added sections 6.8.5 and 6.8.6.
V1.0.1	May. 2025	1) Modify the content of Section 6.5.1 2) Chapter 6.4 adds a description of the X1 oscillator 3) Modify the content of Section 6.7.6
	Jul. 2025	Modify the product structure diagram of CMS32M6734EGH48FA